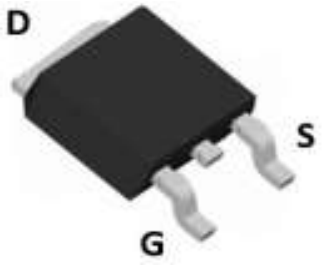
N-Channel Enhancement Mode Field Effect Transistor

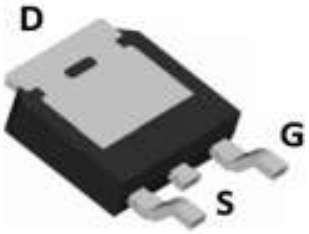
Product Summary

- V_{DS} 60V
- I_D 35A
- $R_{DS(ON)}$(at V_{GS}= 10V) ＜31mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜38mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

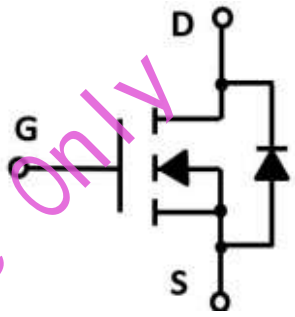
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply





TO-252



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
YC35N06RT	YC35N06RT	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	35	A
	T_C=70℃		27	
Pulsed Drain Current		I_{DM}	120	A
Maximum Power Dissipation	T_C=25℃	P_D	39	W
	T_C=70℃		25	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	3.2	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

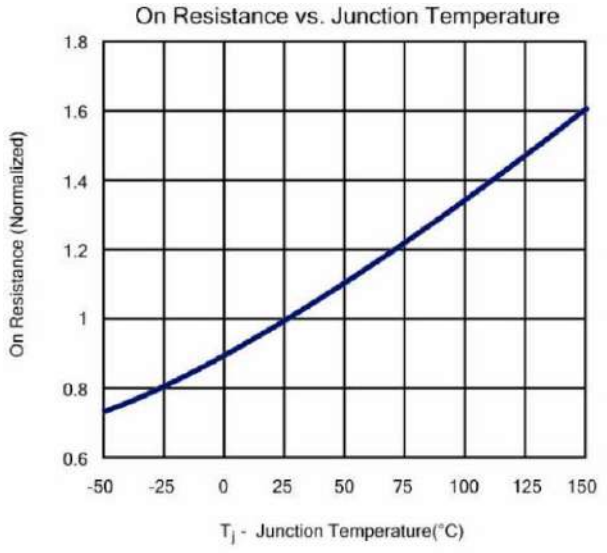
Electrical Characteristics (Tc =25℃ Unless Otherwise Specified)

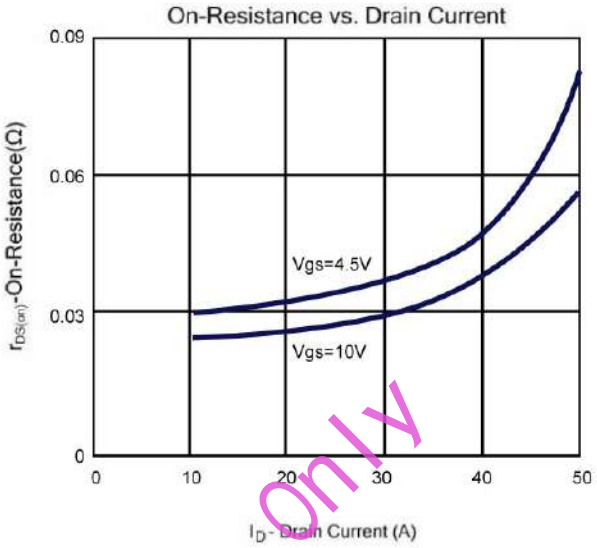
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D=20A		27	31	mΩ
		V_{GS}=4.5V, I_D=16A		31	38	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_D=20A		23		nC
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=4.5V, I_D=20A		12		
Qgs	Gate-Source Charge			4.8		
Qgd	Gate-Drain Charge			6.2		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,f=1MHz		885		pF
Coss	Output Capacitance			98		
Crss	Reverse Transfer Capacitance			30		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.9		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, R_L =1.5Ω, V_{GEN}=10V, R_G=3Ω		12		ns
tr	Turn-On Rise Time			8		
$t_{d(off)}$	Turn-Off Delay Time			43		
tf	Turn-Off Fall Time			4		

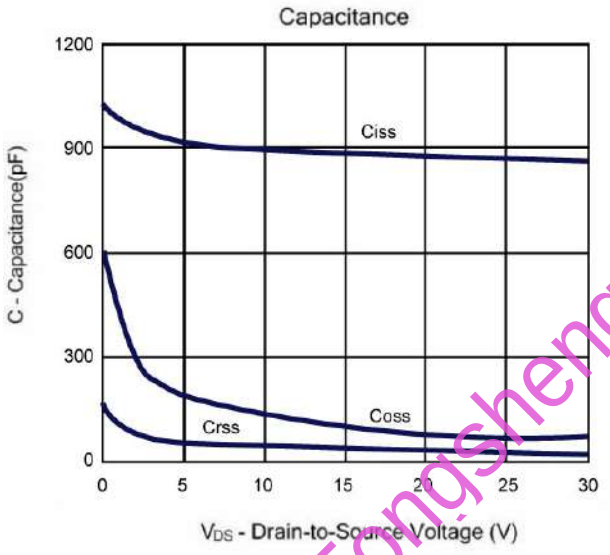
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

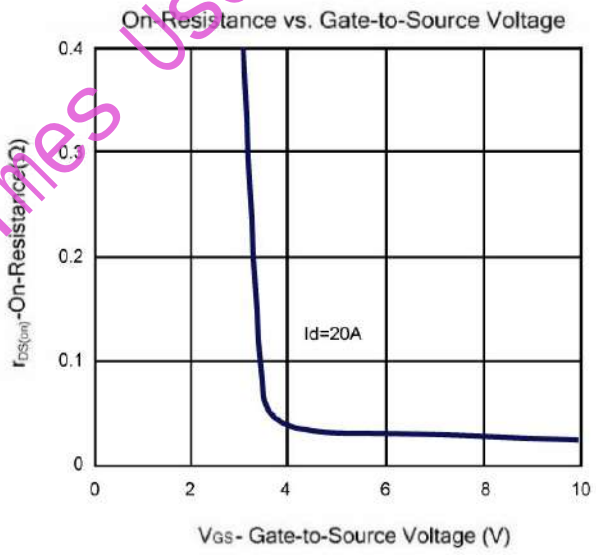
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

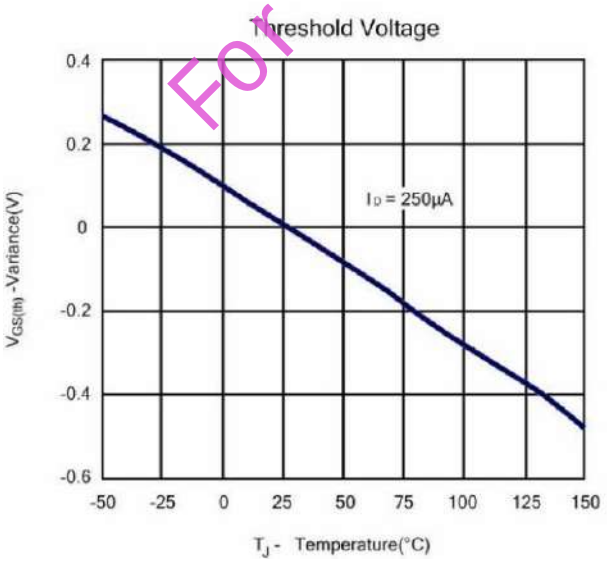
Typical Characteristics (T_J =25℃ Noted)

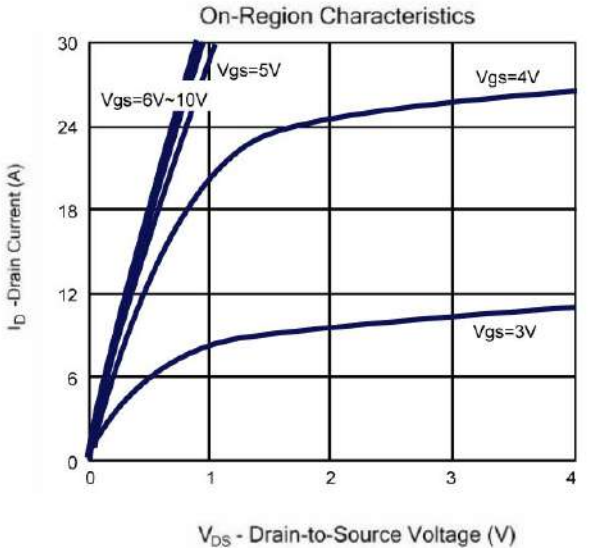






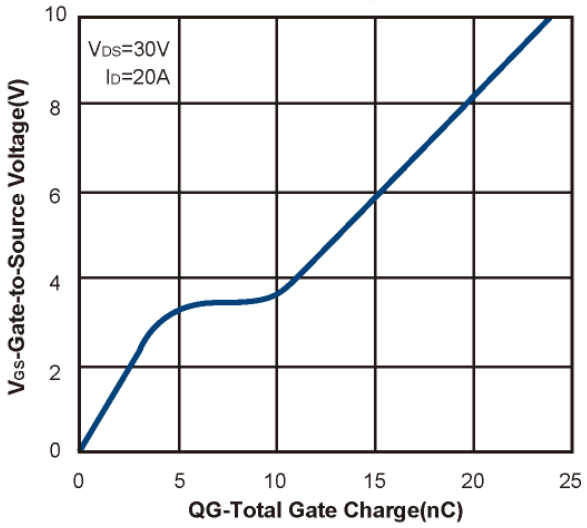




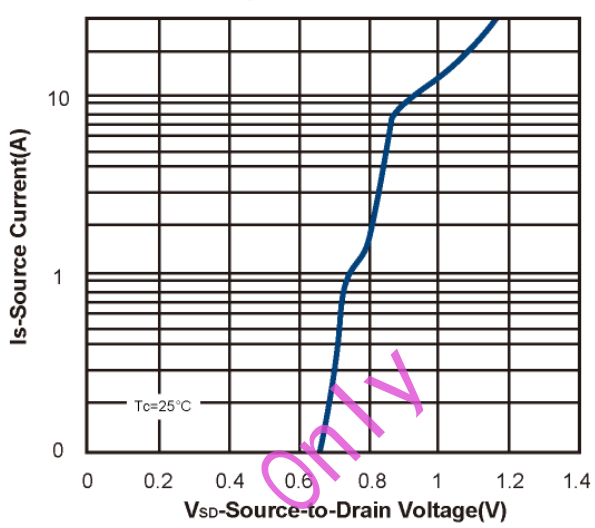


Typical Characteristics (T_J =25℃ Noted)

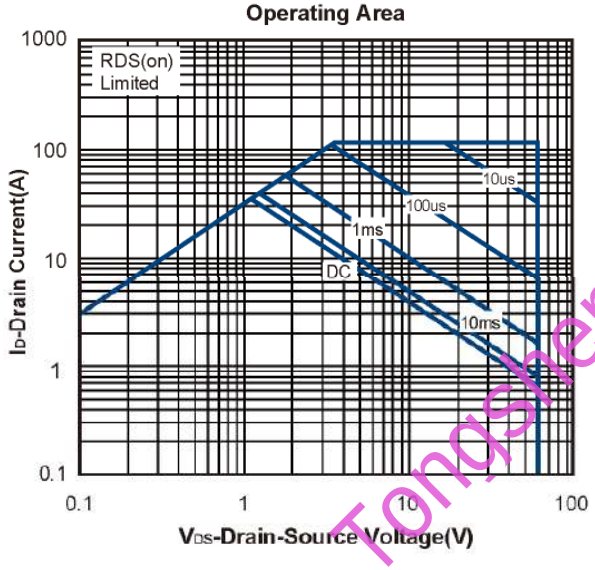
Gate Charge



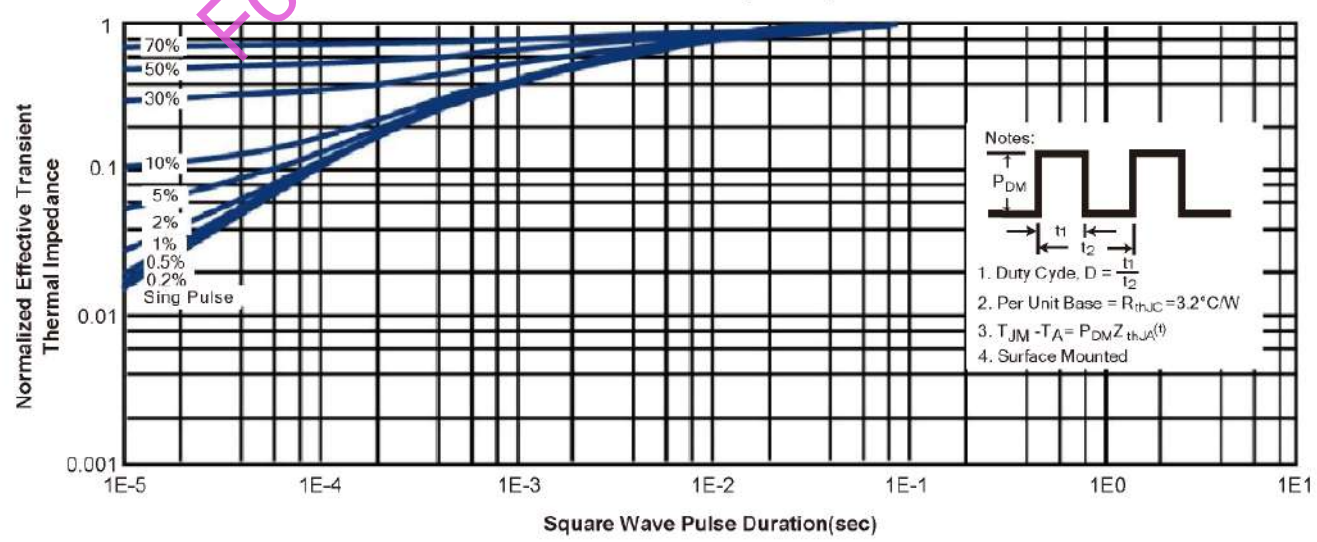
Body-diode characteristics



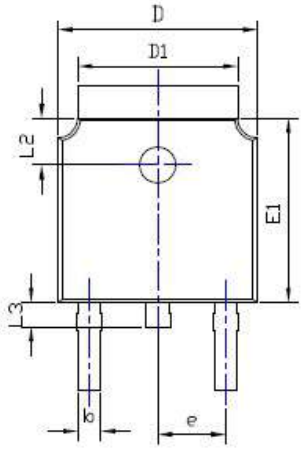
Maximum Forward Biased Safe Operating Area



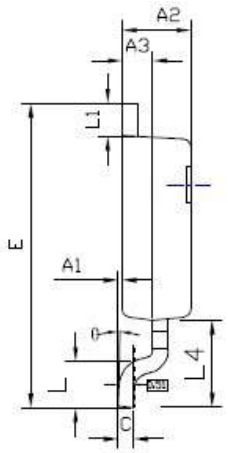
Normalized Thermal Transient Impedance, Junction-to-Case



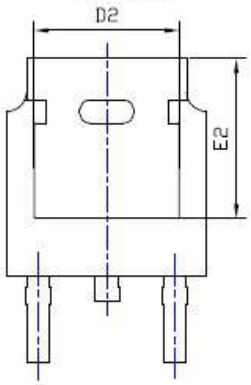
TO-252 Package information



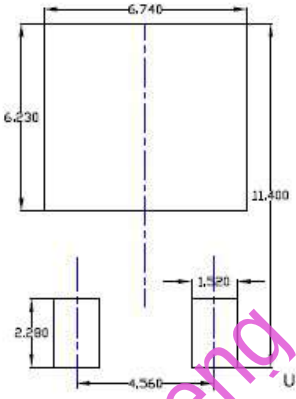
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS						
SYMBOL	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.187	0.193	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Disclaimer

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