

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP6080AG uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

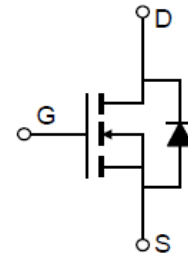
General Features

- $V_{DS} = 60V, I_D = 80A$
- $R_{DS(ON)} < 4.0m\Omega @ V_{GS} = 10V$ (Typ: 3.5m Ω)
- $R_{DS(ON)} < 5.0m\Omega @ V_{GS} = 4.5V$ (Typ: 4.0m Ω)
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

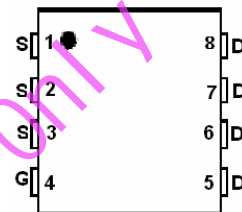
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

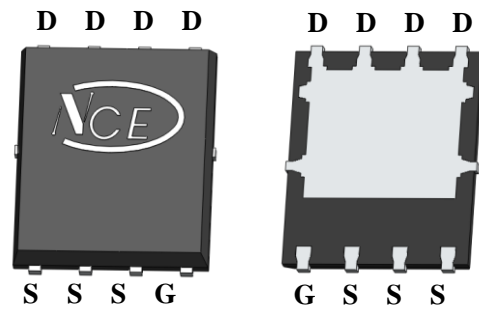
100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



Top View

Bottom View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP6080AG	NCEP6080AG	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	80	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D(100^\circ C)$	58	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	85	W
Derating factor		0.68	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	400	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.47	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

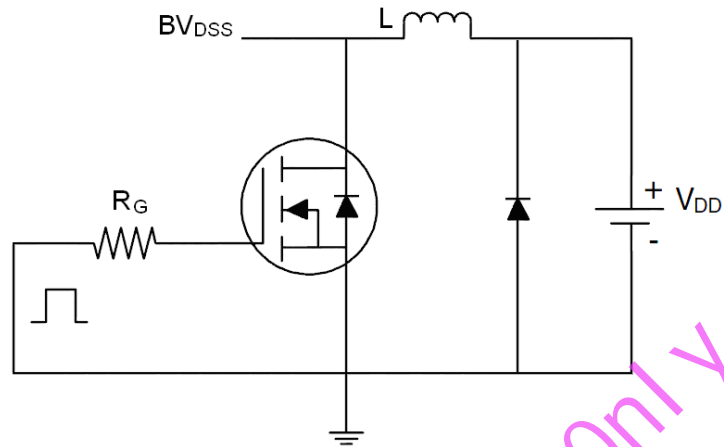
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	3.5	4.0	m Ω
		$V_{GS}=4.5V, I_D=40A$	-	4.0	5.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=40A$	40	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	4000	-	PF
Output Capacitance	C_{oss}		-	680	-	PF
Reverse Transfer Capacitance	C_{rss}		-	23	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=40A$ $V_{GS}=10V, R_G=4.7\Omega$	-	11	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=40A,$ $V_{GS}=10V$	-	67		nC
Gate-Source Charge	Q_{gs}		-	12		nC
Gate-Drain Charge	Q_{gd}		-	8.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=80A$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	80	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ ^(Note 3)	-	48		nS
Reverse Recovery Charge	Q_{rr}		-	60		nC

Notes:

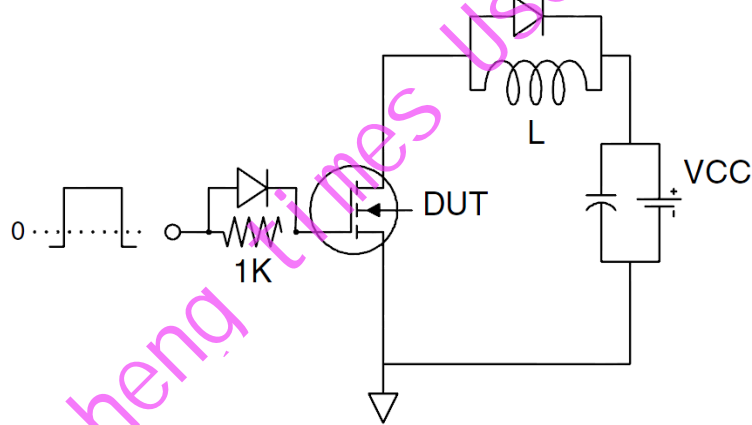
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test Circuit

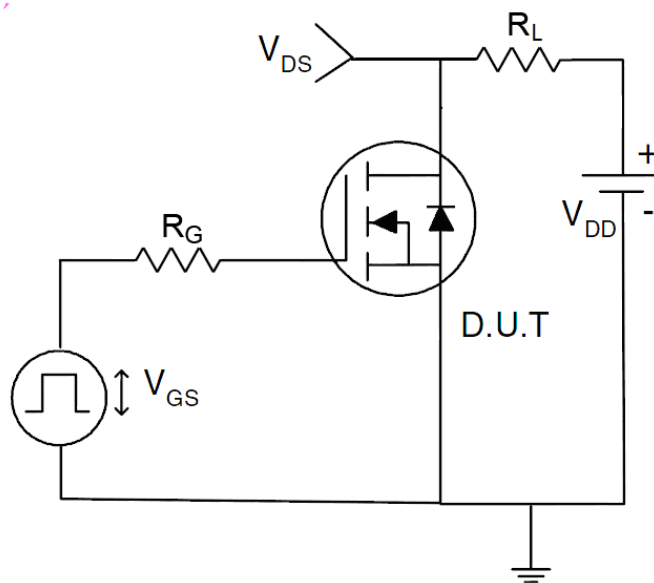
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



For Tongsheng Times Use Only

Typical Electrical and Thermal Characteristics

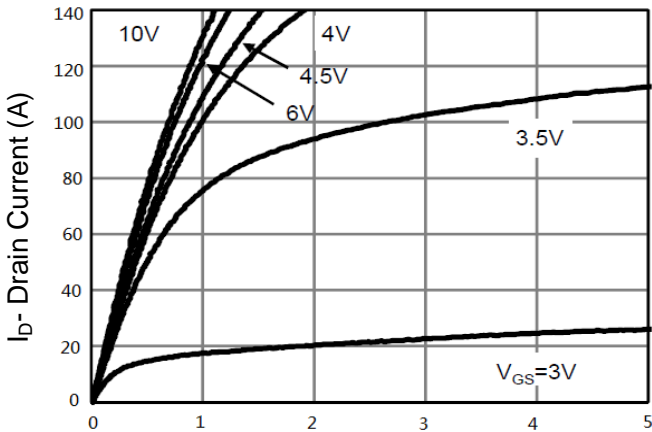


Figure 1 Output Characteristics

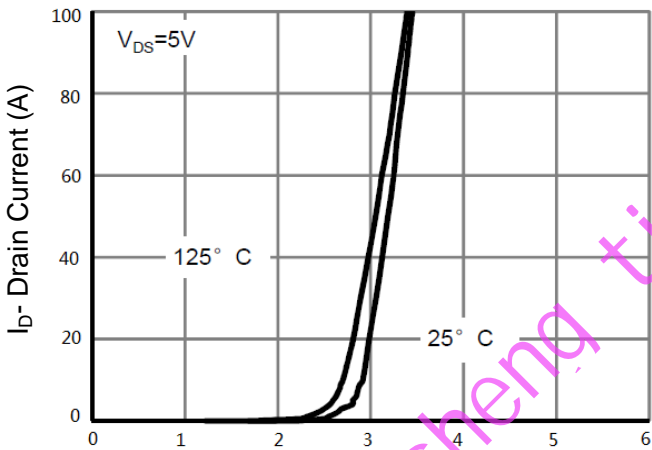


Figure 2 Transfer Characteristics

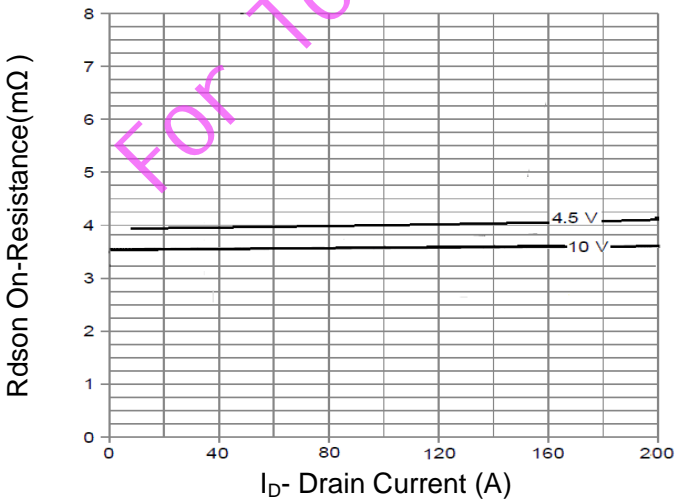


Figure 3 $R_{DS(on)}$ - Drain Current

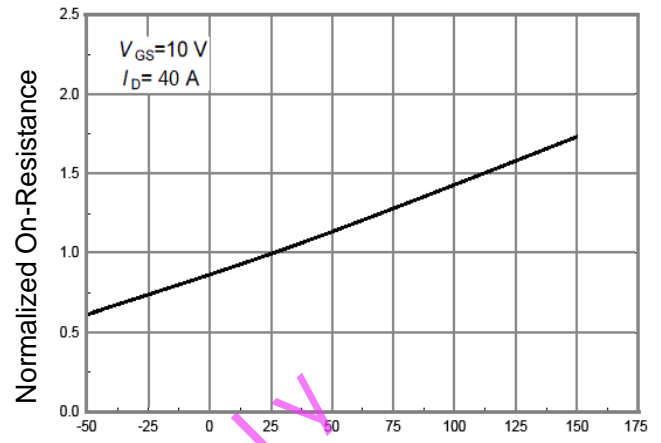


Figure 4 $R_{DS(on)}$ -Junction Temperature

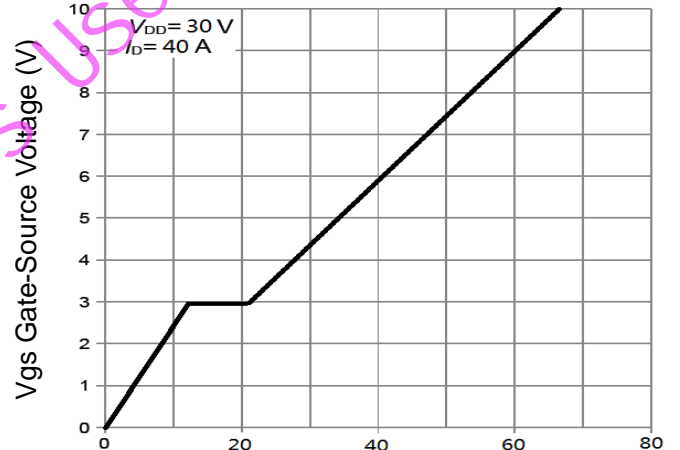


Figure 5 Gate Charge

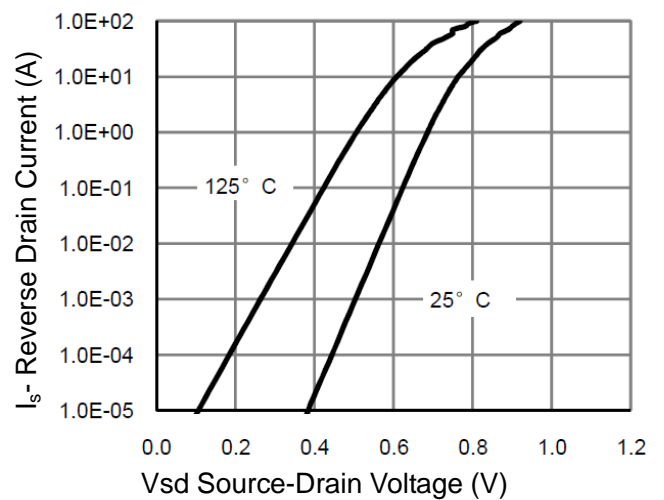


Figure 6 Source- Drain Diode Forward

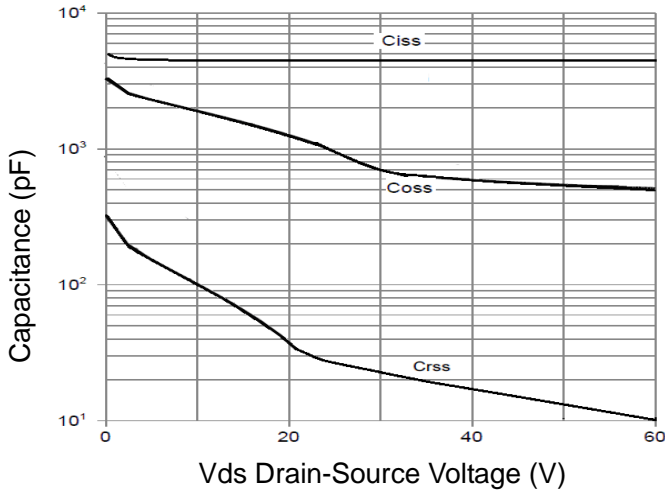


Figure 7 Capacitance vs Vds

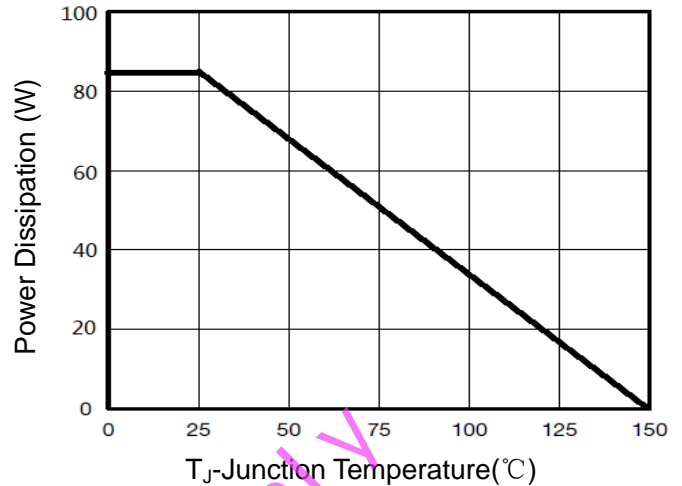


Figure 9 Power De-rating

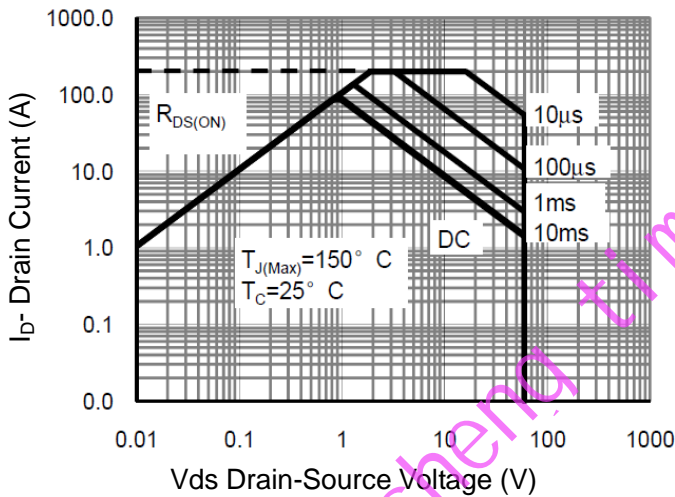


Figure 8 Safe Operation Area

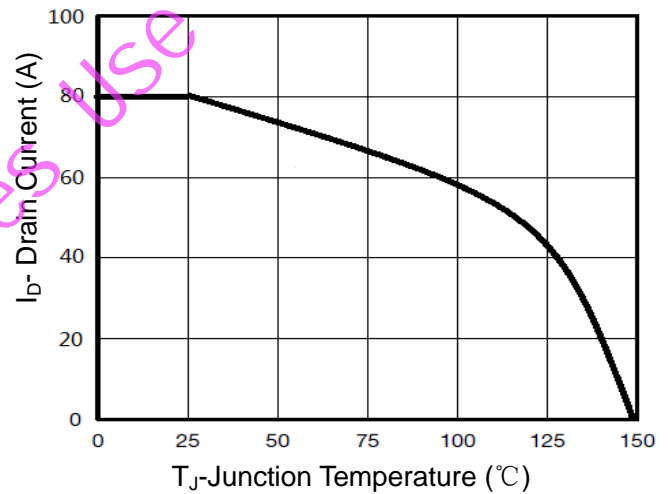


Figure 10 Current De-rating

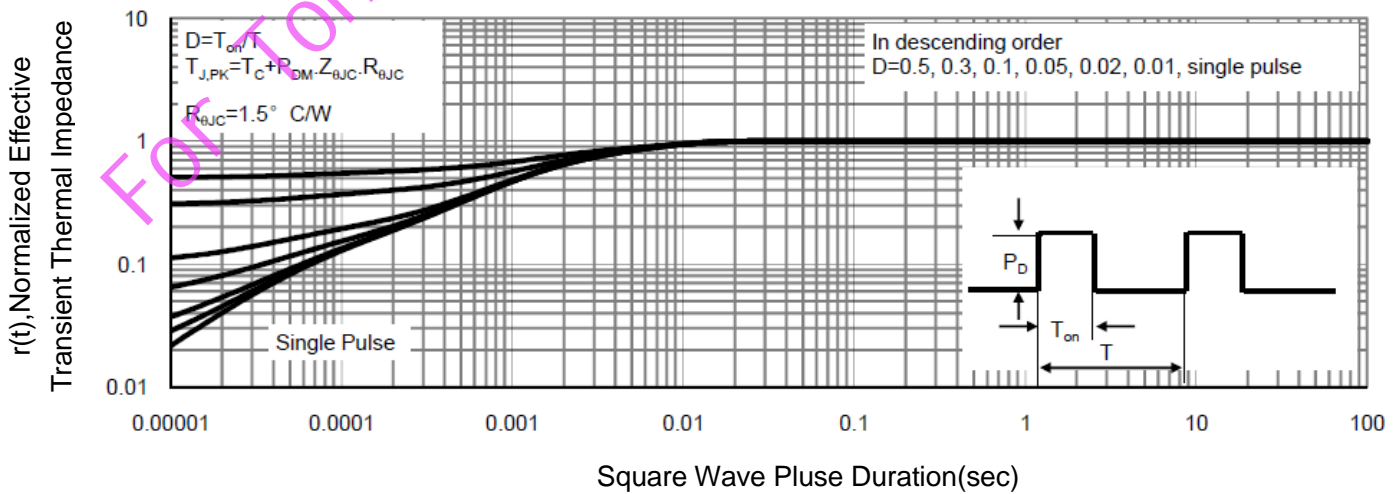
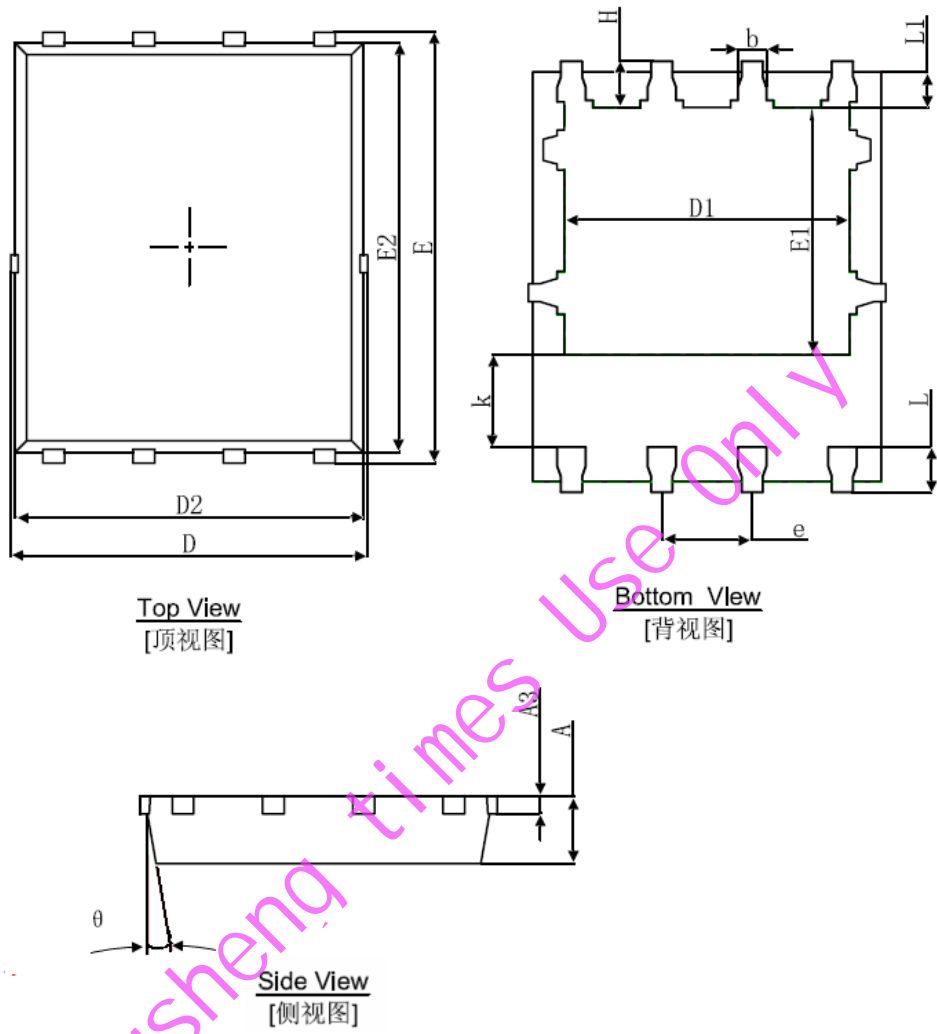


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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