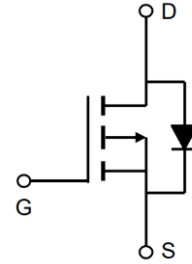


-30V P-Channel Enhancement Mode MOSFET

Description

The AP50P03DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = -30V$ $I_D = -50A$

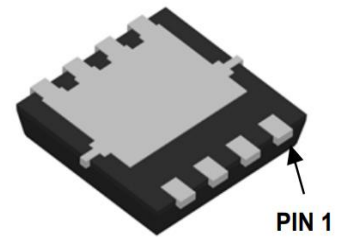
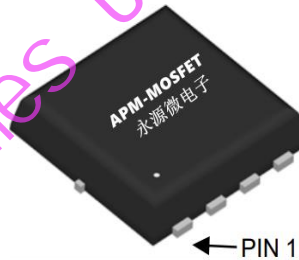
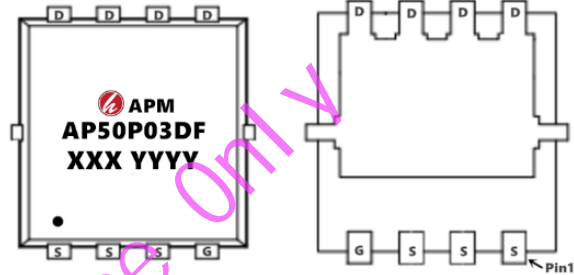
$R_{DS(ON)} < 13m\Omega$ @ $V_{GS} = -10V$ (Type: 8.8m Ω)

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P03DF	PDFN3*3-8L	AP50P03DF XXX YYYY	5000

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	±20	V
$I_{D@TC=25^\circ C}$	Continuous Drain Current, VGS @ -10V1	-50	A
$I_{D@TC=100^\circ C}$	Continuous Drain Current, VGS @ -10V1	-27	A
IDM	Pulsed Drain Current ²	-130	A
EAS	Single Pulse Avalanche Energy ³	125	mJ
IAS	Avalanche Current	-50	A
$PD@TC=25^\circ C$	Total Power Dissipation ⁴	37	W
$PD@TA=25^\circ C$	Total Power Dissipation ⁴	1.67	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
RθJA	Thermal Resistance Junction-Ambient 1	75	°C/W
RθJC	Thermal Resistance Junction-Case1	3.36	°C/W

-30V P-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-34	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.0232	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-30A	---	8.8	13	mΩ
		V _{GS} =-4.5V, I _D =-15A	---	14	20	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	-1.4	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-30A	---	30	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	9	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-15A	---	22	---	nC
Q _{gs}	Gate-Source Charge		---	8.7	---	
Q _{gd}	Gate-Drain Charge		---	7.2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-15A	---	8	---	ns
T _r	Rise Time		---	73.7	---	
T _{d(off)}	Turn-Off Delay Time		---	61.8	---	
T _f	Fall Time		---	24.4	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	2215	---	pF
C _{oss}	Output Capacitance		---	310	---	
C _{rss}	Reverse Transfer Capacitance		---	237	---	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	-42	A
I _{SM}	Pulsed Source Current		---	---	-130	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V
t _{rr}	Reverse Recovery Time	I _F =-15A, dI/dt=100A/μs, T _J =25°C	---	19	---	nS
Q _{rr}	Reverse Recovery Charge		---	9	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、The power dissipation is limited by 175°C junction temperature
- 4、EAS condition: T_J=25°C, V_{DD}= -24V, V_G= -10V, R_G=7Ω, L=0.1mH, I_{AS}= -50A
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

-30V P-Channel Enhancement Mode MOSFET

Typical Characteristics

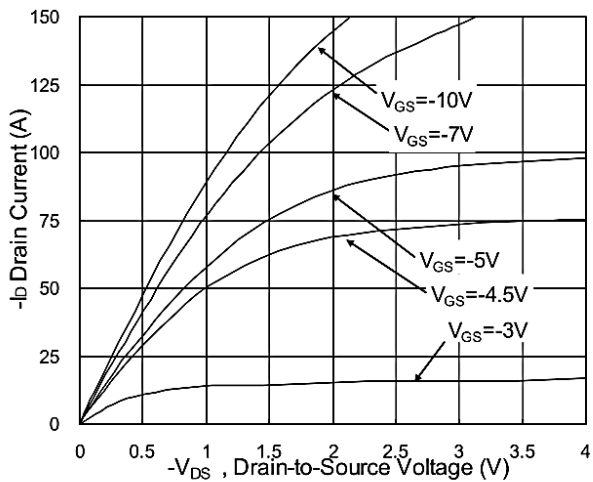


Fig.1 Typical Output Characteristics

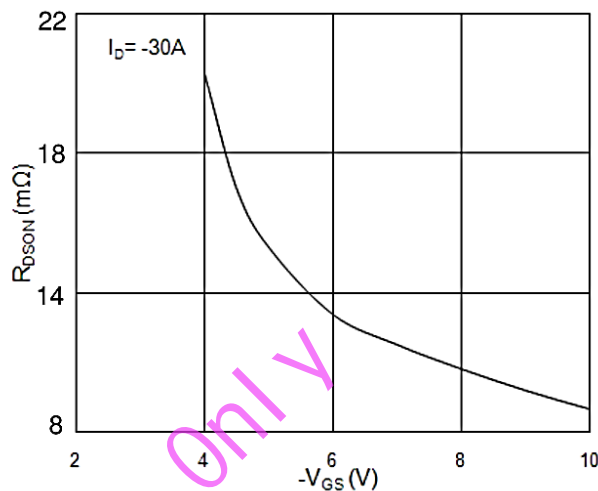


Fig.2 On-Resistance vs. G-S Voltage

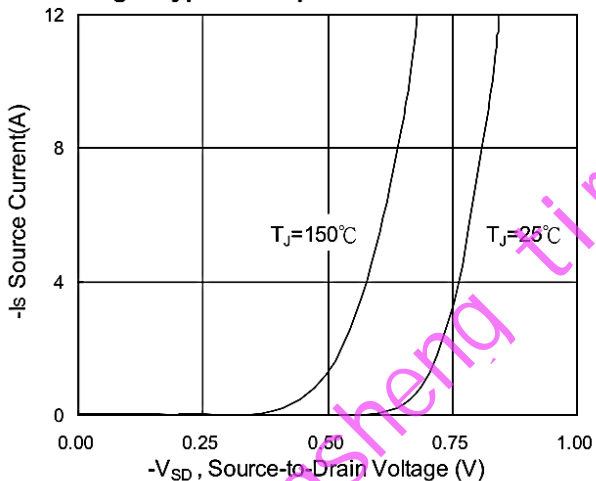


Fig.3 Forward Characteristics of Reverse

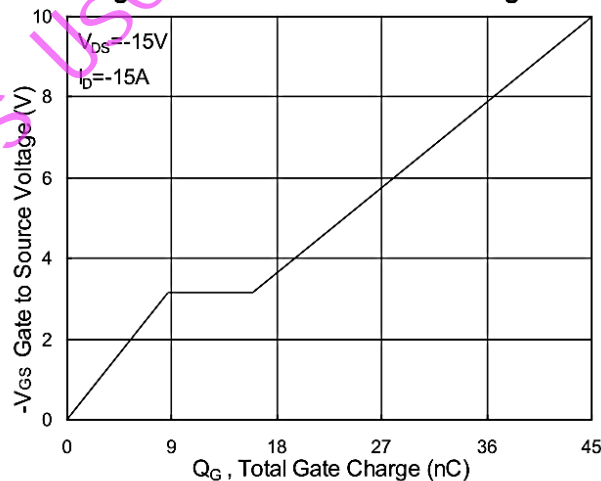


Fig.4 Gate-Charge Characteristics

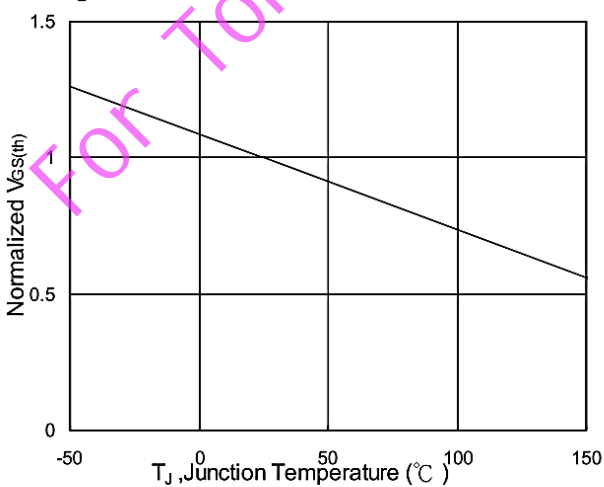


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

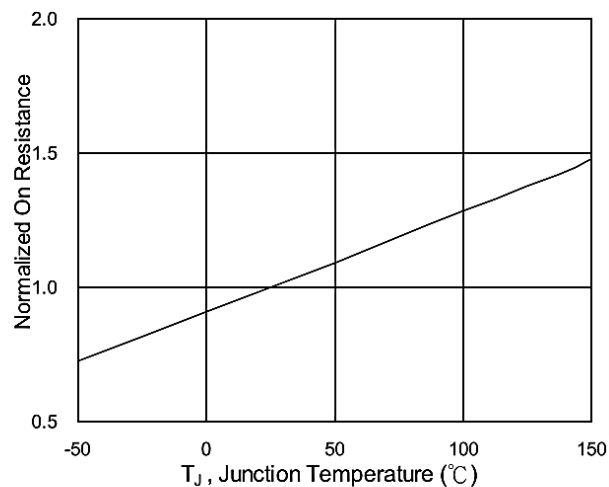


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

-30V P-Channel Enhancement Mode MOSFET

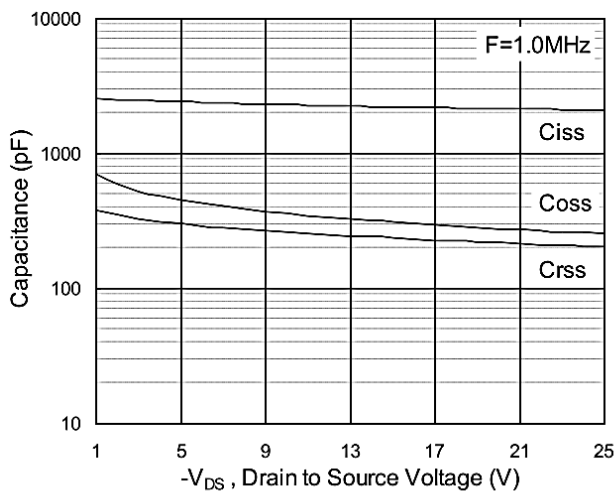


Fig.7 Capacitance

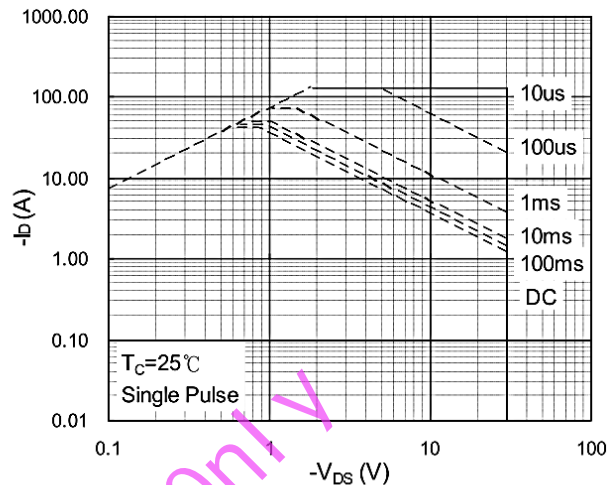


Fig.8 Safe Operating Area

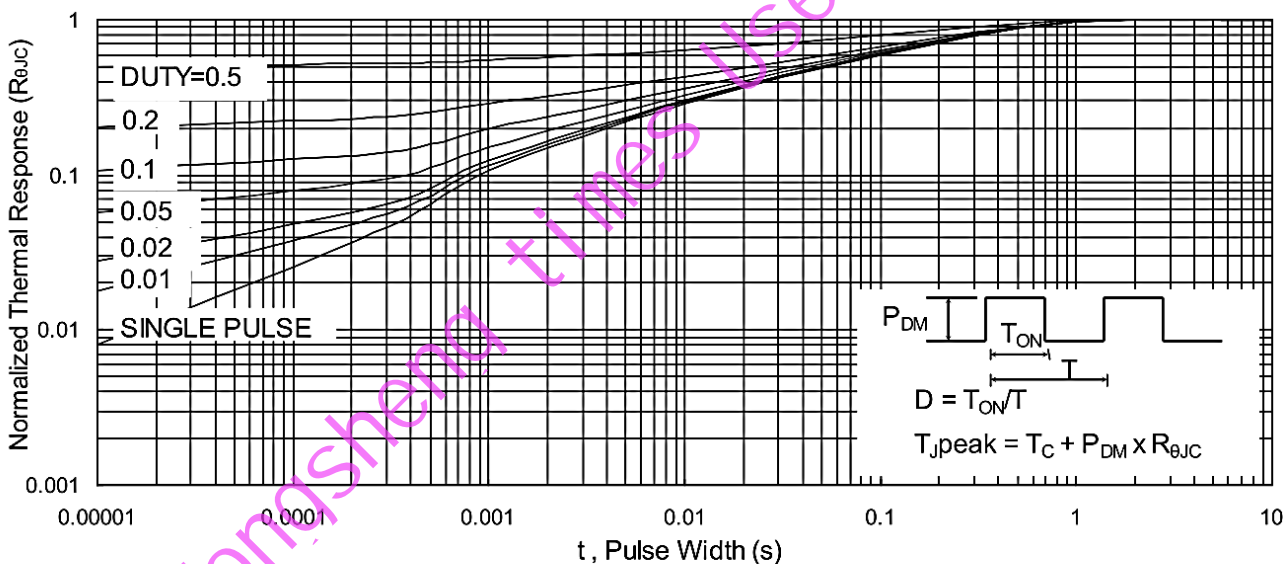


Fig.9 Normalized Maximum Transient Thermal Impedance

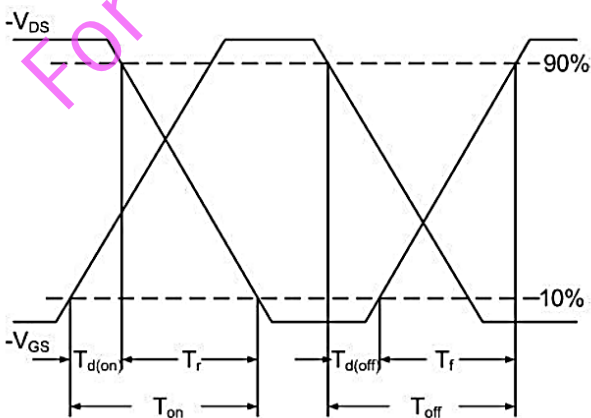


Fig.10 Switching Time Waveform

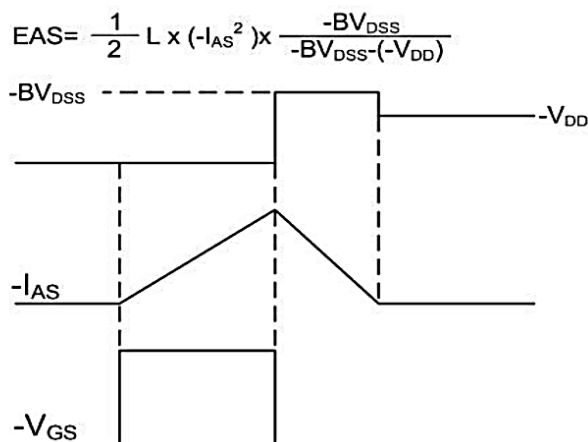
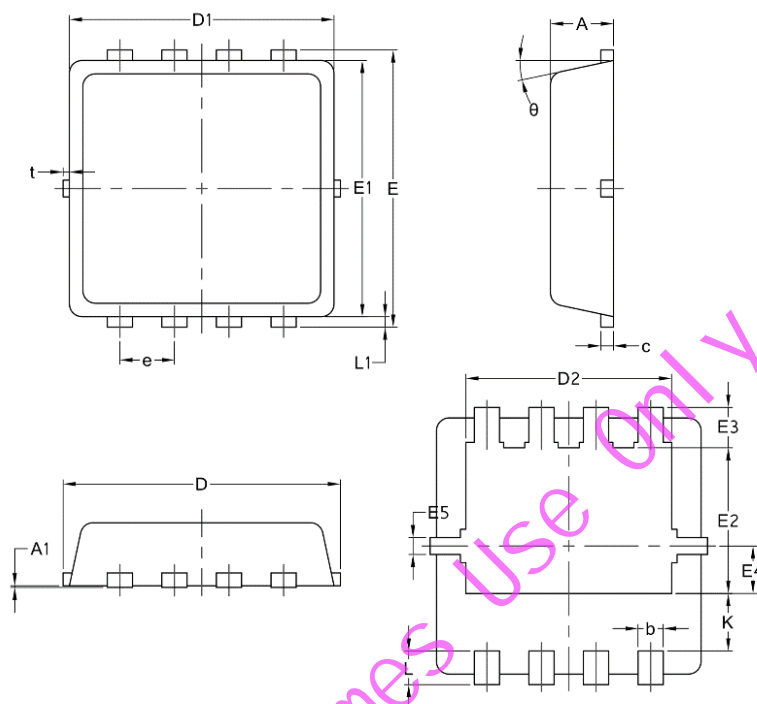


Fig.11 Unclamped Inductive Switching Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$

-30V P-Channel Enhancement Mode MOSFET

Package Mechanical Data-PDFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

-30V P-Channel Enhancement Mode MOSFET

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-30V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve2.0	2020/4/10	Initial release
Rve2.1	2021/9/10	Change of specification forma

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