Advanced Synchronous Rectification Controller

Preliminary Datasheet

FEATURES

- Support CCM, DCM and Quasi-Resonant operation for Switching Mode Power Converter.
- Supports High-Side and Low-Side Configuration, No Auxiliary Winding requirement.
- Typical 50nS Fast Turn-on delay.
- Typical 15nS Fast Turn-off propagation delay.
- Low Forward-drop Regulation Voltage -40mV, minimize the Conduction Losses
- Slew-Rate Detection Prevents False Turn-On from DCM Ringing.
- 1A Source / 5A Sink, Gate Driver Capability.

APPLICATIONS

- Off-line Fly-back / Forward Converter
- USB PD Quick Chargers
- Switching Mode Power Supply

GENERAL DESCRIPTION

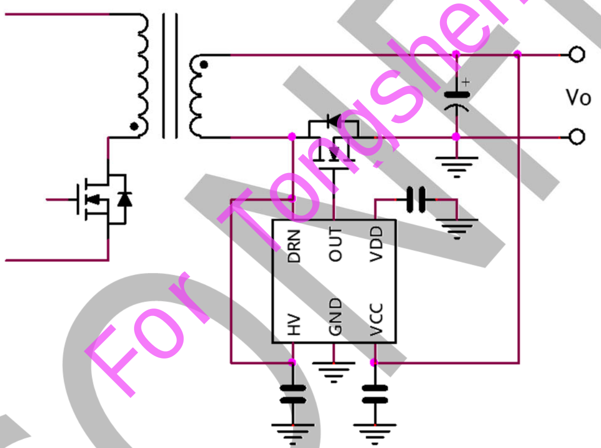
The BT260x family is a synchronous rectification controller IC which support Discontinuous Current Mode (DCM), Continuous Current Mode (CCM) and Quasi Resonant (QR) Mode with driving external low Rd_son MOSFET instead of traditional diode rectifier.

Meanwhile, BT260x support wide output range operation such as 5~20V USB PD adaptors, as well as working even at VCC=0V such as output short circuit circumstance, which prevent thermal concerning from current pass-through the body diode of SR MOSFET. And also supports both High-Side and Low Side Configuration.

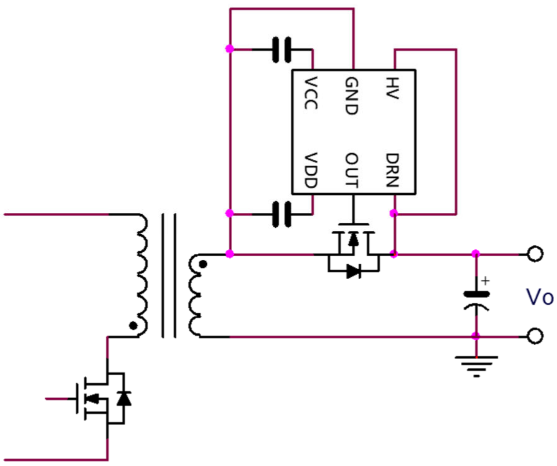
In order to well support CCM operation, BT260x implement stronger Gate Driver ability, as well as extreme short Turn-off propagation delay, thus minimize the switching losses and reverse current.

The BT260x is available in SOT23-6 package

Simplified Application Diagram

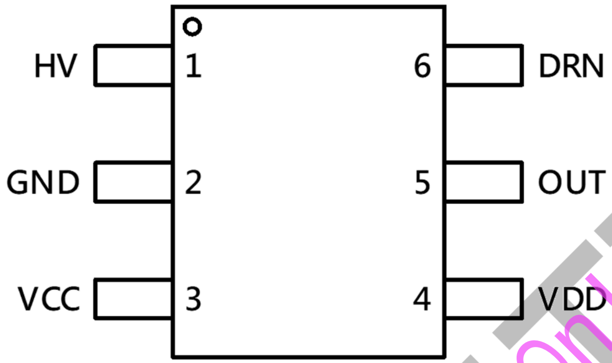


Fly-back with Low-Side SR Configuration



Fly-back with High-Side SR Configuration

PIN ASSIGNMENT



SOT23-6

PIN DESCRIPTIONS

Name	Pin No SOT23-6	DESCRIPTION
HV	1	High-Voltage current source charging input.
GND	2	Ground, connect to MOSFET Source Terminal.
VCC	3	VCC power supply for SR low side application to reduce SR IC power consumption.
VDD	4	LDO output, connect a capacitor to GND.
OUT	5	Driver Output, Connect to MOSFET Gate Terminal.
DRN	6	Connect to MOSFET Drain Terminal.

Part Number	Package	Temp. Range
BT2601	SOT23-6	-40°C to 85°C
BT2602	SOT23-6	-40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

Pin No. SOT23-6	Name	BT2601 MIN	BT2601 MAX	BT2602 MIN	BT2602 MAX	UNIT
1	HV	-1.0	130	-1.0	130	V
2	GND					
3	VCC	-0.3	18	-0.3	40	V
4	VDD	-0.3	6.5	-0.3	6.5	V
5	OUT	-0.3	18	-0.3	10	V
6	DRN	-1.0	130	-1.0	130	V

- Junction Temperature .... 150°C
- Lead temperature (Soldering, 10sec) .... 260°C
- Operating Junction Temperature .... -40°C to 125°C
- Storage Temperature Range .... -65°C to 150°C
- Package Thermal Resistance, θ_{JA} (SOT23-6) (1) .... 206°C/W
- Power Dissipation@ T_A = 25°C (SOT23-6) (2) 0.56W
- ESD Voltage Protection, HBM (Human Body Mode) .... ±2KV
- ESD Voltage Protection, MM (Machine Mode) .... ±200V
- ESD Voltage Protection, CDM (Charged Device Mode) .... ±500V
-

Caution:

Stresses beyond those ratings listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Rating” condition for extended periods may affect device reliability.

Note:

(1) Tested per JEDEC51-3 standard at T_A = 25°C
(2) Calculated in accordance with junction temperature T_J = 125°C

Electrical Characteristics

T_A = +25°C, unless otherwise noted

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
VDD pin							
Turn on Level	VDD_on	V_{DD} Rising		3.5	3.7	3.9	V
Turn off Hysteresis				0.1	0.2	0.3	V
VDD Regulation Voltage	VDD	HV=12V, Fsw=100KHz	BT2601	5.3	5.6	5.9	V
			BT2602	5.7	6.0	6.3	V
Operating Current	iVCC	VCC=8.5V, C_{Load}=2.2nF, Fsw=100KHz,	BT2601		2.3	3.0	mA
	iVDD	VDD=6V, C_{Load}=2.2nF, Fsw=100KHz,	BT2602		1.7	2.5	mA
Quiescent Current	$I_{Q(VDD)}$	V_{DD}=5V, DRN=5V			200	250	uA
Shutdown Current	$I_{SD(VDD)}$	V_{DD}=UVLO-0.1V, DRN=5V			100	120	uA
VCC pin							
VCC Regulation Voltage	VCC	HV=12V, fsw=100KHz	BT2601	8.0	8.5	9.0	V
Max Charging Current	iCCchg	VCC=10V, VDD=4V	BT2602	10	20		mA
VCC Charges VDD threshold		HV=12V, VCC rising	BT2602	4.1	4.4	4.7	V
		Hysteresis		0.1	0.3	0.5	V
HV pin (High Voltage Charge)							
HV Max Charging Current	iHVchg	HV=30V, VCC=7V	BT2601	50	70		mA
		HV=30V, VDD=4V	BT2602	50	70		mA

Electrical Characteristics

T_A = +25°C, unless otherwise noted

Parameter	Symbol	Condition		Min	Typ	Max	Units
DRN pin (SR detection)							
Turn-on threshold	VDSon	DRN – GND		–140	–100	–60	mV
Turn-on delay	TDon	CLoad = 2.2nF			50	70	nS
Minimum Turn-on time	Ton_min			0.75	1.1	1.45	µS
VDS Forward Regulation	VDSreg	GND – DRN		–50	–40	–30	mV
Turn-off Threshold	VDSoff	GND – DRN		–6	–3	0	mV
Turn-off propagation delay(1)					15		nS
Turn-off blanking threshold	VBoff	Ton < Ton_min		1.0	1.5	2.0	V
DRN pin (Slew Rate detection)							
Turn-on Slew Rate detection	Tslew	Sensing DRN=1.5V to –100mV		25	35	45	nS
OUT pin (Gate driver)							
Rising Time	Tr	CLoad = 2.2nF	BT2601		40	60	nS
			BT2602		25	40	
Falling Time	Tf	CLoad = 2.2nF	BT2601		10	20	nS
			BT2602		8	16	
OUT High Level	OUT_Hi	BT2601		VCC–0.1		VCC	V
		BT2602		VDD–0.1		VDD	V
OUT Low Level	OUT_Lo				0.01	0.02	V
Anti-Floating Impedance				43	86	129	KΩ
Pull-Low Impedance		2.4V < VDD < 3.6V	BT2601		2	3	Ω
			BT2602		1	2	Ω
OUT Pre-Clamp (1)		HV = DRN = 100KHz 10V/0V D = 50% OUT tied to HV via 10K-ohm				1	V

NOTE:

(1) Guaranteed by characterization and design.

Functional Overview

The BT260x is a Sync-Rectification Controller IC Family which supports DCM CCM and QR mode operation. The controller generates the conduction interval by means of drain-to-source voltage sensing (VDRN) control algorithm.

The SR MOSFET is turned on when VDRN (DRN to GND) rapidly falls below turn-on threshold -100mV (typical), and is turned off when VDRN reaches above -3mV(typical). The SR conduction voltage drop is continuously monitored and regulated VDRN by -40mV(typical) to overcome the turn-off too early challenge so that to further improve efficiency. Meanwhile, the extremely fast turn-off comparator with ~15nS propagation delay and stronger driving circuit (1A/5A) ensures the fast turn-off of the SR MOSFET in order to well support CCM operation.

Functional Block Diagram

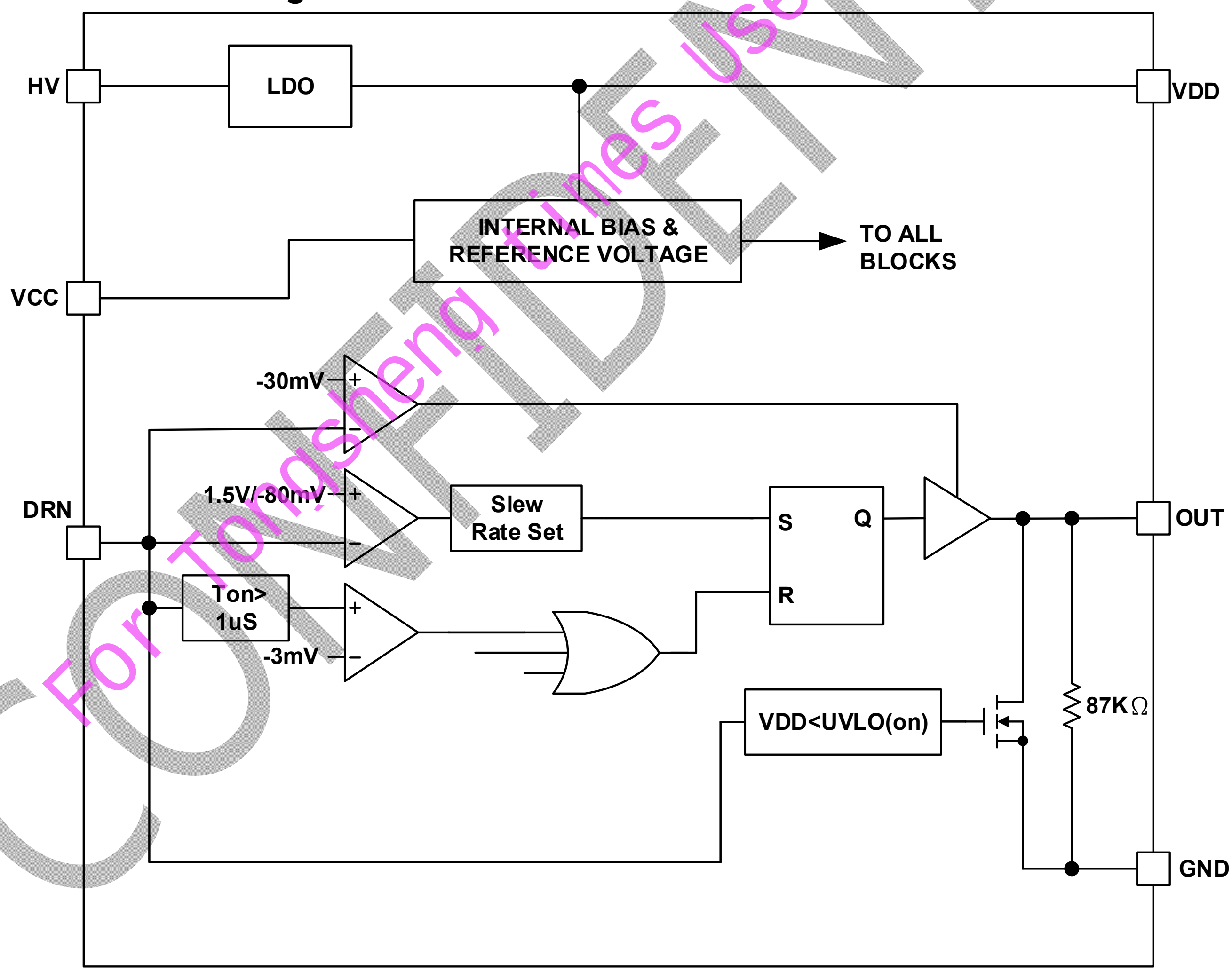


Figure-1.

VDD Generation

BT2601

The BT2601 can be powered by charging the capacitor at VDD.

When system power up, the initial switching pulses at HV charges VCC cap until VCC regulated at typical 8.5V, at same time, the VCC charges the VDD cap as well until VDD regulated at typical 5.5V.

Besides, VCC also can be input by external DC supply, such as 12Vout, at this moment, once VCC>8.5V, the HV pin will no longer charge VCC, under the circumstances reduce HV charge losses can be expected.

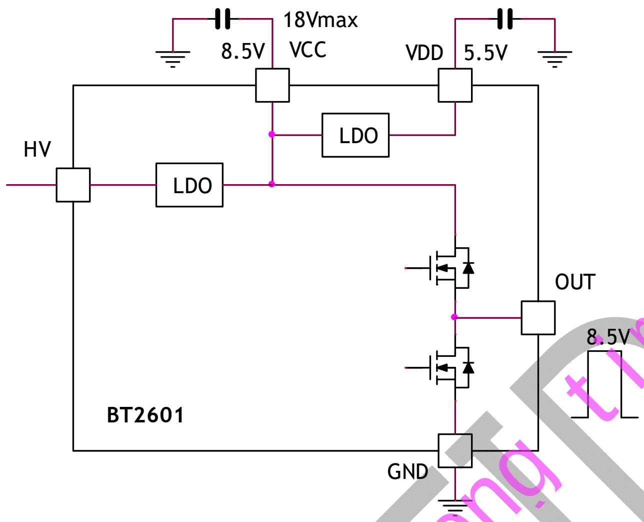


Figure-2.

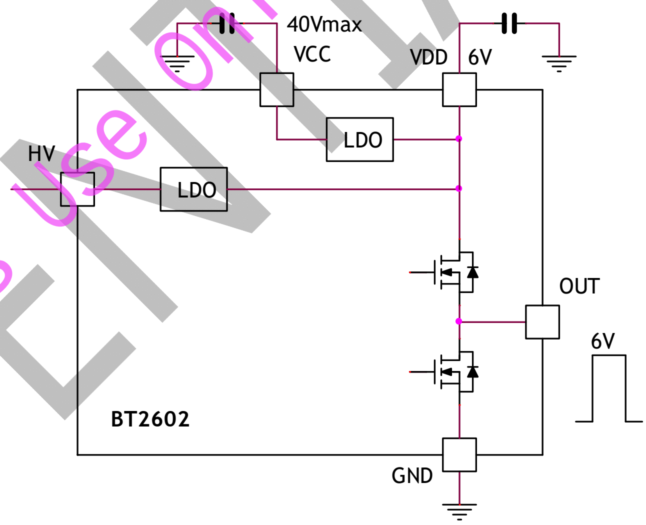


Figure-3.

BT2602

The difference from BT2601 is that BT2602 can be powered by charging the capacitor at VDD either form HV or VCC, in other words, the BT2602 has dual supply input which has flexible design for user to support PD wide output voltage up to 20V.

However, when system power up, the initial switching pulses at HV will charge VDD cap directly with max 70mA capability until VCC regulated at typical 6V.

Besides, VCC also can be input pin by external DC supply up to 40Vmax, at this moment, once VCC > 4.4V typical, then HV Current Source will be disconnected in order to reduce power losses, so that VCC will supply and regulated VDD at typical 6V.

Start-Up and Under-Voltage Lockout (UVLO)

When VDD rises above VDD_on 3.7V (typical), the BT260x controller is enabled to operate. Once VDD falls below Under-Voltage-Lockout (UVLO) 3.5V typically, the BT260x enters shutdown mode, and OUT pin is kept low.

Turn-On Control

BT2601x operates by sensing DRN to GND forward voltage, when DRN drop below ~1.5V, the internal slew rate detection timer will be enabled, when VDRN drop reaches -100mV(typ) before the timer end, the OUT pin will allow to drive the SR MOSFET with Ton_delay time typical ~50nS.

In a case of DRN drop reaches -100mV after the timer end, such as detects a DCM Ringing with low slew-rate, thus controller will keep OUT low to prevents SR MOSFET turn-on from false condition.

Minimum On Time (Ton_min)

When initially body diode of the SR MOSFET is conducted first, the DRN waveform can generate high-frequency ringing due to parasitical factor, the ringing may large enough to false trigger the Turn-off threshold -3mV(typ), see Figure-4., to prevent this happen, BT260x controller built-in a blanking feature which also be called Ton_min, when the SR MOSFET turns on, the control circuit will keep on state continues for a specific period. Therefore, the Ton_min prevents a false turn-off from DCM Ringing, see Figure-5. However, in case of VDRN reaches 1.5V(typ) within the Ton_min, OUT will be pulled low immediately.

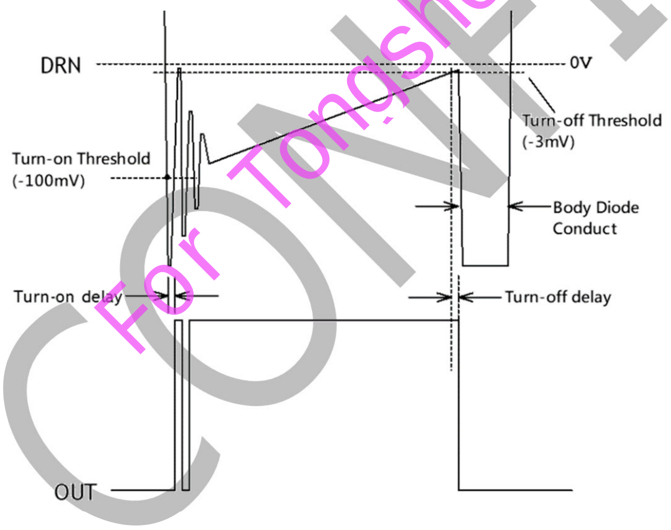


Figure-4.

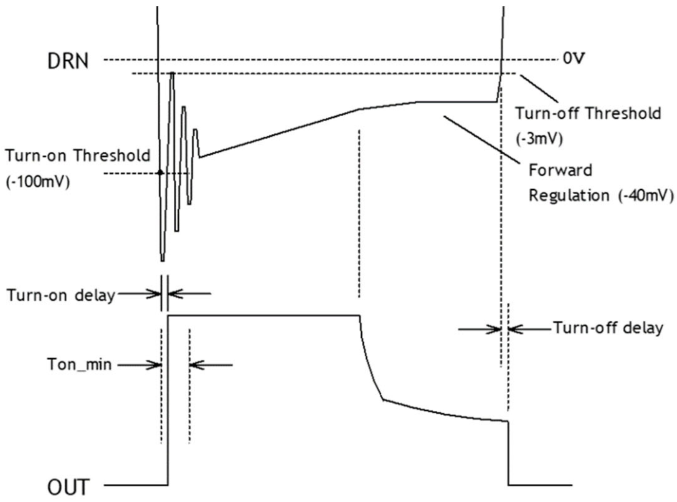


Figure-5.

Forward Regulation

After gate driver turns-on the SR MOSFET, when VDRN rises to reach the forward voltage drop -40mV(typ) due to the decreasing of the switching current, the BT260x controller decreases the gate voltage level in order to enlarge the on resistance of SR MOSFET, see Figure-3.

With this control algorithm, VDRN is regulated by typically -40mV, even when the current through the SR MOSFET down to very low. This feature regulates the gate driver voltage at lower level (linear area) to prevent the SR MOSFET turns off too early, and meanwhile which has benefit to speed up the turn-off time which is critical in CCM operation.

CCM SR Challenge

When converter operates in CCM condition, primary side controller is dominating the switching cycle sequence, while primary HV-FET turns-off moment, secondary current iD doesn't rise immediately before primary HV-FET Drain voltage reach above Vbulk DC level, so, there is no Cross-Conduction concern at this moment.

As to primary HV-FET turns-on scenario, that's another story, since the primary side controller is dominating the switching cycle sequence, HV-FET always turns-on first then transfer to secondary iD turns-off, therefore, without a doubt, primary side current id and secondary side current iD can overlap at that transition, see Figure-6, so there is high risk can happen Cross-Conduction between PWM driver on-state and SR driver off-state transition.

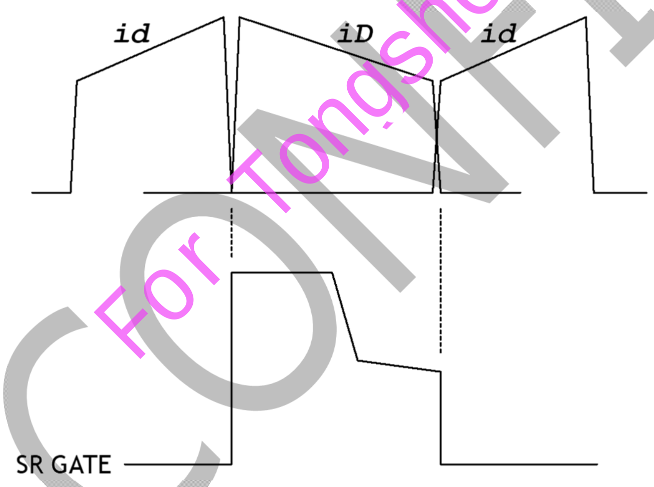


Figure-6.

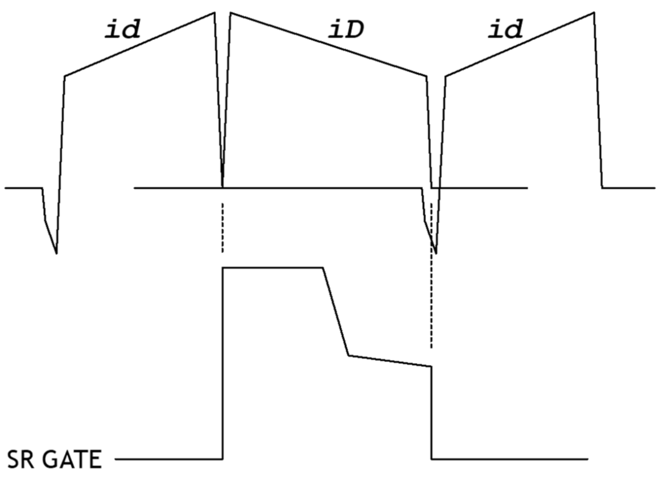


Figure-7.

In order to avoid Cross-Conduction happen, here are the ways:

(1) Very strong driving sink current.

(2) Very short turn-off propagation delay time.

(3) Choose SR MOSFET with smaller Qg.

(4) Decrease the PWM driver source current, to slow-down the HV MOSFET turn-on speed.

(5) Increase SR MOSFET parasitical inductance to get additional offset voltage to turn-off SR MOSFET premature.

(6) Implement VDRN forward regulation feature to lower the gate voltage to speed up the turn-off time.

However, these ways may result in additional cost / limit the design flexibility and increase power loss….

BaiGong's Total Solution, A New Breakthrough:

In order to totally resolve the Cross-Conduction issue, to adopt BT120x product family together with BT260x as total solution is recommended, see BT120x family datasheet for detail.

Since the BT1200 family is a Novel CCM-ZVS Flyback PWM controller, a ZVS delay time can be created between PWM id current and SR iD current, there is no overlap anymore, see Figure 7, the Cross-Conduction issue can be free, totally safe, saving cost and improve system efficiency you can have both.

Turn-Off Control

After SR MOSFET turns-on, as soon as VDRN rises to trigger the turn off threshold -3mV (typ), the gate voltage is pulled to zero immediately after a very short turn-off propagation delay of typical 15ns.

Turn-Off Blanking

As soon as the gate driver OUT is pulled up to 0V by DRN reaching the turn-off threshold (-3mV), a turn-off blanking time is enabled, during which the gate driver signal is latched-off. The turn-off blanking would be removed once DRN rises above 1.5V typically, then controller will reset gate driver from latch-off, a new cycle can be start.

Slew-Rate Detection

In DCM operation, the DCM ringing at DRN may drop below 0V. If DRN ringing reaches the turn-on threshold, SR controller will false turn-on if controller has no any detection feature.

BT260x has built-in Slew Rate Detection feature prevents the false turn-on from DCM Ringing.

External Resistor on DRN and HV pins

The device may be damaged when Over-Voltage occurred, so application designs must be done appropriately to guarantee safe operation, especially on the DRN and HV pin.

A common over-voltage condition is that when the body diode of the SR MOSFET is turned on, the forward voltage drop may exceed the negative rating on Drain and HV pin. In this case, place an external resistor from Drain terminal of the MOSFET to DRN and HV pin of the controller is must. User needs to check real system waveform to secure SR controller working safe. Generally, the resistance 300Ω~1KΩ is recommended for DRN pin, and 50Ω~200Ω is recommended for HV pin.

System Application Information:

Below are the applications information for Fly-back Converter.

1. Low-Side SR Configuration:

Figure-8 shows the BT2602 application in which the VCC supply derived from the output voltage (VOUT), it is available in a wide output range such as PD 0~20V by BT2602 has VCCmax=40V rating. To place a small resistor such as 2-Ohm on VCC rail is recommended to filter out the ripple noise from Vout of power converter. HV is connected with Drain of SR MOSFET, in this configuration, when Vout ≥ 5V, VCC pin dominates the charging VDD and HV pin stops charging so therefore reducing the supply losses; when Vout < 4.4V(typ) such as 3.3V / 2.5V or even short to ground, HV pin will take over to charging VDD to keep BT2602 working at those condition.

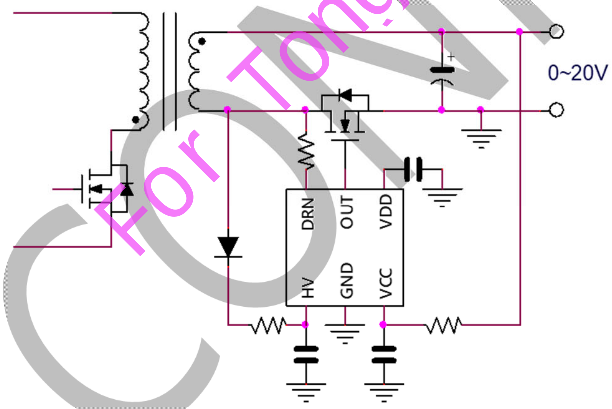


Figure-8. BT2602 Low Side

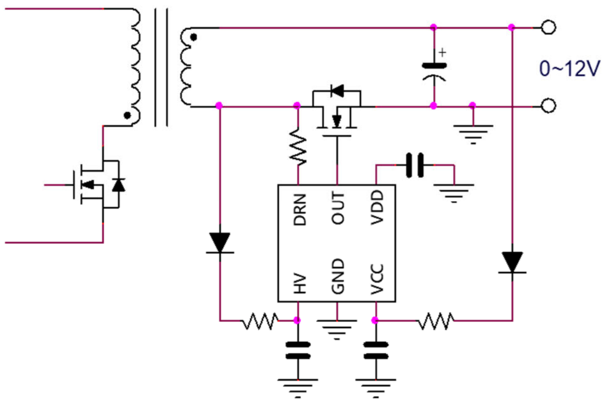


Figure-9. BT2601 Low Side type-1

For BT2601 Low-Side application, there are 3 types reference applications here:

Type-1: Figure-9 shows the BT2601 Low-Side type-1 configuration, in which VCC is supplied from Vout, and HV pin is supplied from Drain of SR MOSFET, since BT2601 VCC has 18V max rating, such configuration is recommended for 0~12V output range, because considering OVP≈15V is possible. Meanwhile, since HV pin is supplied from Drain of SR MOSFET, when VCC < 8V or even Vout short to ground, HV will keep charging the VCC to regulate at 8.5V (typical), therefore, place a diode on VCC rail is required to avoid VCC pin be pulled down to ground when Vout is shorted to ground happens.

Type-2: Figure-10 is BT2601 Low-Side type-2 Configuration in which the device supply totally from HV pin, so therefore output voltage range can be 0~20V, this is a cost-effective configuration.

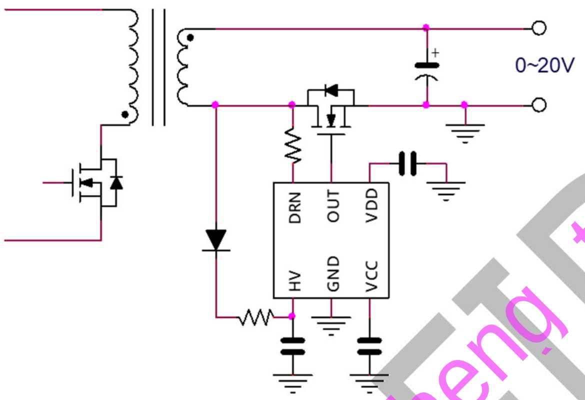


Figure-10. BT2601 Low Side type-2

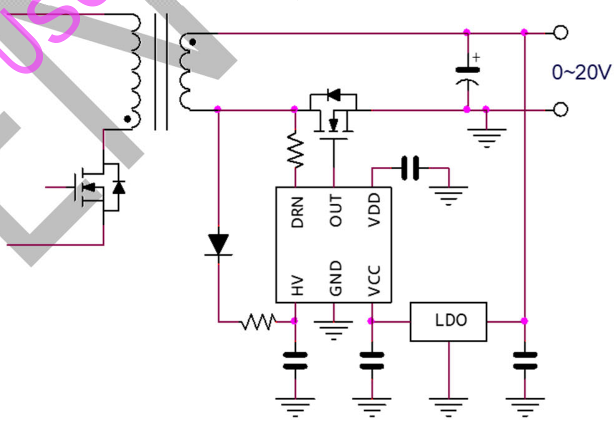


Figure-11. BT2601 Low Side type-3

Type-3: Figure-11 shows another way to support Vout=0~20V range as BT2601 Low-Side type-3 configuration, compare with type-2 configuration, the type-3 VCC supplied from Vout via additional linear regulator, this way helps to reduce supply losses to further improve the SR conversion efficiency.

2. High-Side SR Configuration:

Figure 12 and Figure 13 are showing the BT2601/02 in which configured as High-Side Sync-Rectification.

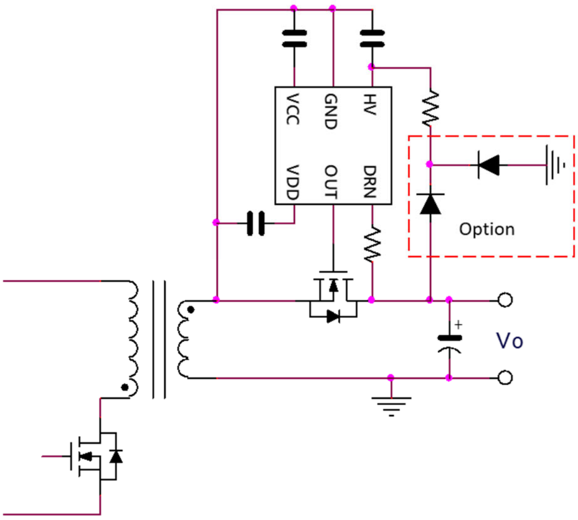


Figure-12. BT2601/02 High-Side SR_1

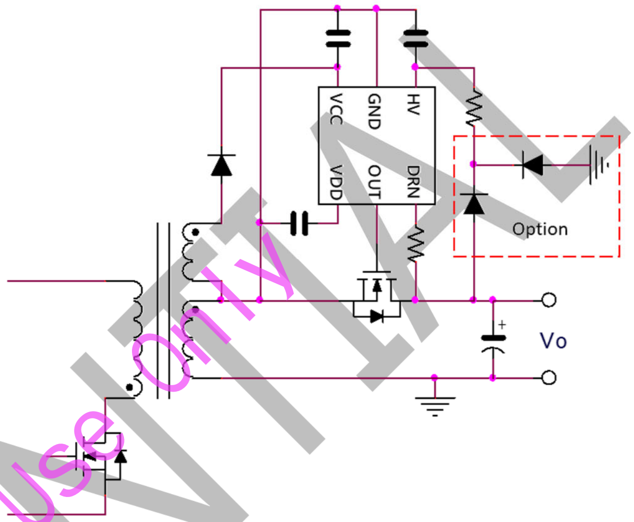


Figure-13. BT2601/02 High-Side SR_2

In Figure-12 configuration, BT2601/02 HV pin can be supplied from Vout or GND which is alternative supply-rail, this is a cost-effective solution without the need of additional winding.

In Figure-13 configuration, VCC is supplied by additional winding, please be noted that the VCC max rating is: 18V for BT2601, and 40V for BT2602.

Compare with Fig-12, the Fig-13 with lower supply losses, so the higher efficiency is expected.

PCB Layout Consideration

Care needs to be taken of the PCB Layout is to minimize the current loop areas and track lengths, whatever using single-layer or multi-layer.

Guideline

- Keep the ceramic bypass capacitor MLCC as close as possible cross VDD/VCC to GND.
- The DRN-pin6 and GND-pin2 sense points requires very short track lengths and keep loop area as small as possible to prevent the stray inductance is added to the SR-MOSFET package inductance, as this will result in additional offset voltage which tends to turn off the SR-MOSFET prematurely.
- Connecting the DRN-pin6 directly to the SR-MOSFET drain pad to prevent the offset voltage across the stray inductance in the SR drain current path.
- Connecting the GND-pin2 directly to the SR-MOSFET source pad to prevent the offset voltage across the stray inductance in the SR-MOSFET source current path. Because this trace shares both the gate driver path and the SR-MOSFET Drain sensing path, it is recommended to make this trace as short as possible.
- Make the gate driver loop as small as possible with running parallel tracks from OUT-pin5 and GND-pin2 to the SR MOSFET, to minimize the stray inductance.
- Careful and keep the DRN-pin6 sensing loop far away from the transformer winding power loop to prevent the interrupting from each other.

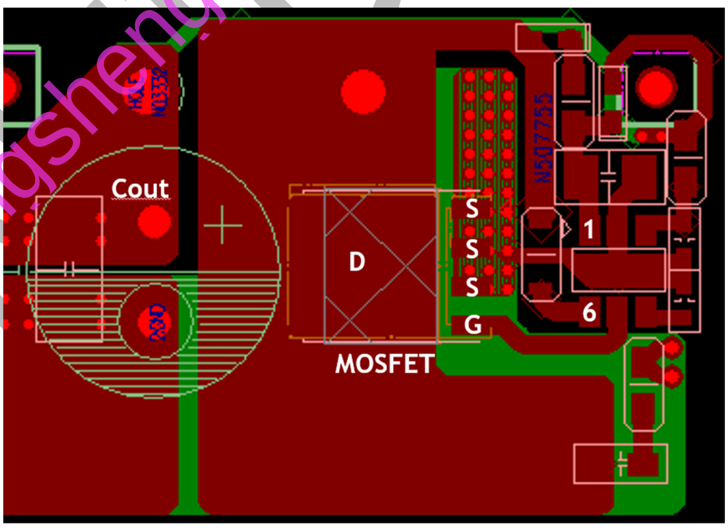
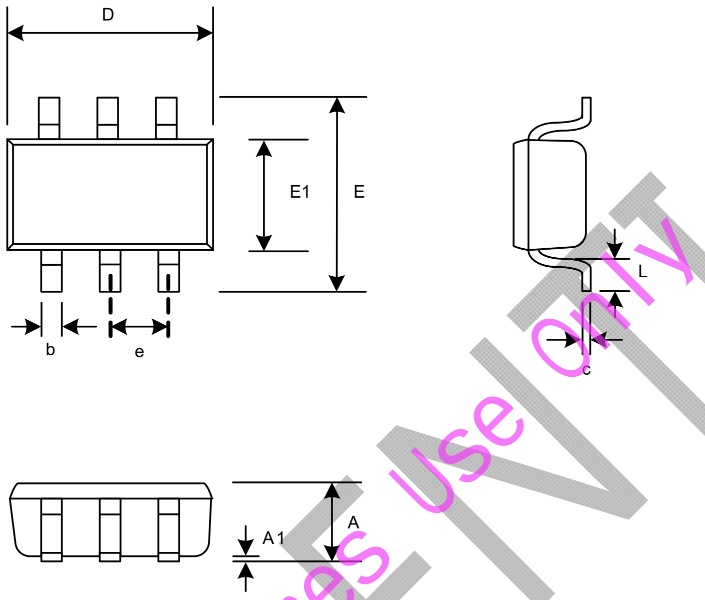


Figure 14. PCB Layout Example

PACKAGE INFORMATION

SOT23-6



Symbols	Dimensions			
	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.889	1.450	0.031	0.057
A1	0.000	0.152	0.000	0.006
b	0.250	0.560	0.010	0.022
c	0.080	0.254	0.003	0.010
D	2.692	3.120	0.106	0.123
E	2.591	3.000	0.102	0.118
E1	1.397	1.803	0.055	0.071
e	0.838	1.041	0.033	0.041
L	0.300	0.610	0.012	0.024

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