JW1572

Offline Boost PFC CV Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW1572 is a constant voltage controller with high voltage accuracy which applies to single stage boost power factor correction (PFC) applications. Constant on time control strategy ensures high power factor, and the input voltage detection circuit is not needed, which simplifies the system design and saves the loss.

Critical conduction mode operation reduces the switching losses, improves the EMI performance and largely increases the efficiency.

JW1572 has multi-protection functions which largely enhance safety and reliability of the system, including VCC UVLO, CS short current protection (SCP), FB over voltage protection, 2nd OVP and over temperature protection.

JW1572 is available in SOP8 package.

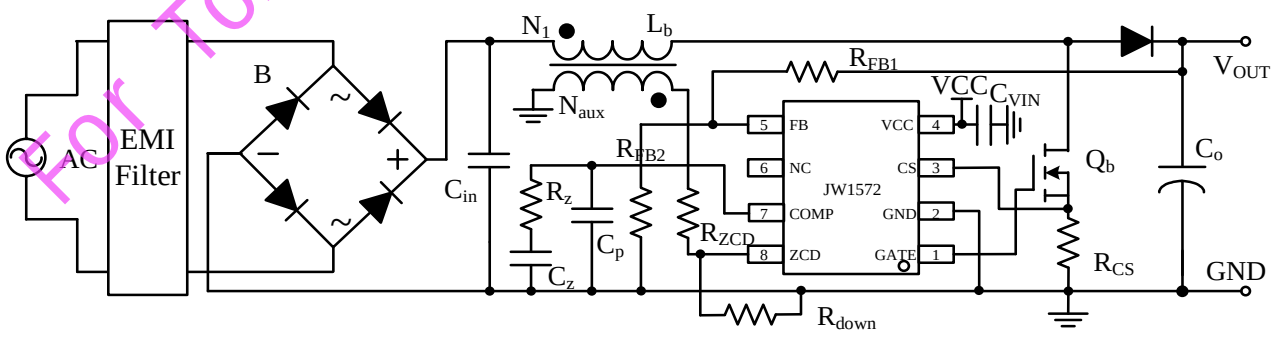
FEATURES

- Low Quiescent Current
- +0.6A/-1.4A Peak Gate Drive Current
- High Power Factor and Low THD
- Critical Conduction Mode
- High Reference Voltage Accuracy
- High Efficiency over Wide Operating Range
- Reduce Frequency at Light Load
- Open Feedback Protection
- Disable Function
- Cycle by Cycle Current Limit by CS Voltage
- Internal over Temperature Protection
- 2nd OVP
- SOP8 Package

APPLICATIONS

- SMPS
- AC-DC Adapter
- Flat TV

TYPICAL APPLICATION



JW1572 PFC Application

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1572SOPB#TR	SOP8	JW1572 YW□□□□□	Green

Notes:

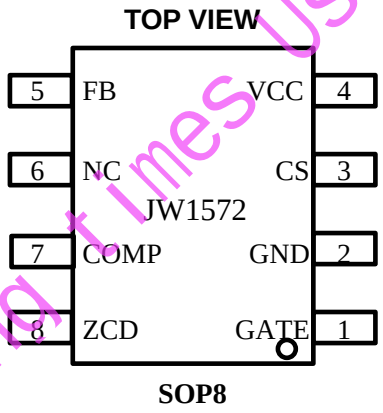
1) JW□□ #TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VCC..... -0.3 to 45V
ZCD..... -0.6 to 45V, -0.7 to -0.6V<100μs
CS, COMP.....-0.3 to 5.5V
FB.....-0.3 to 5V, 5 to 6V<100ms
GATE.....-0.3 to 13V
Junction Temperature[2)]..... 150ºC
Lead Temperature..... 260ºC
Storage Temperature..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model).....2kV

RECOMMENDED OPERATING CONDITIONS

VCC..... 10 to 40V

Operating Junction Temperature (T_J) [3]..... -40ºC to 125ºC

THERMAL RESISTANCE[4]

	θ_{JA}	θ_{JC}
SOP8	120	60ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1572 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_J= -40°C to 125°C, typical values shown are for T_J = 25°C, unless otherwise stated

Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Management						
VCC Start-up Voltage	V_{CC_ST}		10.45	11	11.95	V
VCC Under Voltage Lockout	V_{CC_UVLO}		7.5	8.2	8.9	V
VCC Operation Current	I_{VCC_OP}	$f_{sw}=F_{MIN}$, GATE Floating	200	300	400	μA
VCC Start-up Supply Current	I_{VCC_ST}	$V_{CC}= V_{CC\_ST}$-1V	14	21.5	30	μA
VCC Supply Current during Green Mode	I_{VCC_GM}	V_{CC}=16V, V_{FB}=0V	30	50	70	μA
Current Limit(CS Pin)						
CS Cycle by Cycle Limit Voltage	V_{CS_MAX}		0.35	0.4	0.45	V
Leading Edge Blanking Time	T_{LEB2}	0.4V<V_{CS}<1.5V	240	300	360	ns
SCP Voltage	V_{CS_SCP}		1.4	1.5	1.6	V
Leading Edge Blanking Time of SCP	T_{LEB1}	V_{CS}>1.5V	190	250	310	ns
Feedback and OVP(FB Pin)						
FB Reference Voltage	V_{FB_REF}		2.45	2.5	2.55	V
OVP Threshold of FB	V_{FB_OVP}		2.56	2.68	2.80	V
FB OVP Hysteresis	$V_{FB\_OVP\_HYST}$		0.1	0.2	0.28	V
FB Start-up Voltage	V_{FB_ST}		0.34	0.4	0.46	V
FB Ipeak Start-up Voltage	$V_{FB\_PK\_ST}$		2.18	2.3	2.41	V
FB Ipeak Stop Voltage	$V_{FB\_PK\_STOP}$		2.28	2.4	2.52	V
FB Ipeak Voltage Hysteresis	$V_{FB\_PK\_HYST}$		0.05	0.1	0.15	V
Compensation(Comp pin)						
Transconductance	G_m	$\|V_{FB}-V_{FB\_REF}\|$≤50mV	8.85	13.9	19.3	μA/V
Source Current of COMP	I_{SRC_COMP}	V_{FB}=0V, V_{comp}=1.6V	18.41	21.26	24.11	μA
Sink Current of COMP	I_{SINK_COMP}	V_{FB}=2.6V, V_{comp}=1.6V	0.82	1.3	1.78	μA
Maximum Clamp Voltage of COMP	V_{comp_max}	V_{FB}=2.0V	2.49	2.6	2.87	V
Minimum Clamp Voltage of COMP	V_{comp_min}	V_{FB}=2.6V	0.41	0.64	0.88	V
PFC on Timer and Frequency Foldback						
Maximum On-time of GATE	T_{MOT}		28.5	33	37.5	μs

T_J= -40°C to 125°C, typical values shown are for T_J = 25°C, unless otherwise stated Advance Information, not production data, subject to change without notice.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Maximum Switching Frequency	F_{MAX}		130	140	149	kHz
Minimum Switching Frequency	F_{MIN}	V_{FB}=2.6V, V_{CS}=1V	20.2	23	25.8	kHz
Driver(GATE Pin)						
Gate High Voltage	V_{GS_H}		10	11.5	13	V
Maximum Source Current[5)]	I_{SRC_GATE}	GBD, GATE=0V	/	0.6	/	A
Maximum Sink Current[5)]	I_{SINK_GATE}	GBD, GATE=4V	/	1.4	/	A
Demagnetization Sense(ZCD Pin)						
Demagnetization Time-out	T_{DEM_MAX}		38	44	50	μs
Valley Sense(ZCD Pin)						
Valley Sense Threshold[5)]	dv/dt	GBD	/	12.8	/	V/μs
Demagnetization sense low level[5)]	V_{ZCD_L}	GBD	-100	-90	-80	mV
Demagnetization sense high level[5)]	V_{ZCD_H}	GBD	-10	0	10	mV
Blanking time of ZCD	T_{delay}		494	630	766	ns
Valley Sense Time-out[5)]	T_{valley}	GBD	/	3.8	/	μs
2nd OVP Threshold	I_{OVP2}		1.15	1.3	1.45	mA
Fault Reset Delay Time	T_{FRD}	SCP and 2nd OVP Fault	645	720	815	ms
Internal OTP						
Internal over Thermal Protection Threshold[6)]	T_{OTP}	GBD	/	140	/	℃
Internal over Thermal Protection Hysteresis[6)]	T_{OTP_HYST}	GBD	/	30	/	℃

Note：

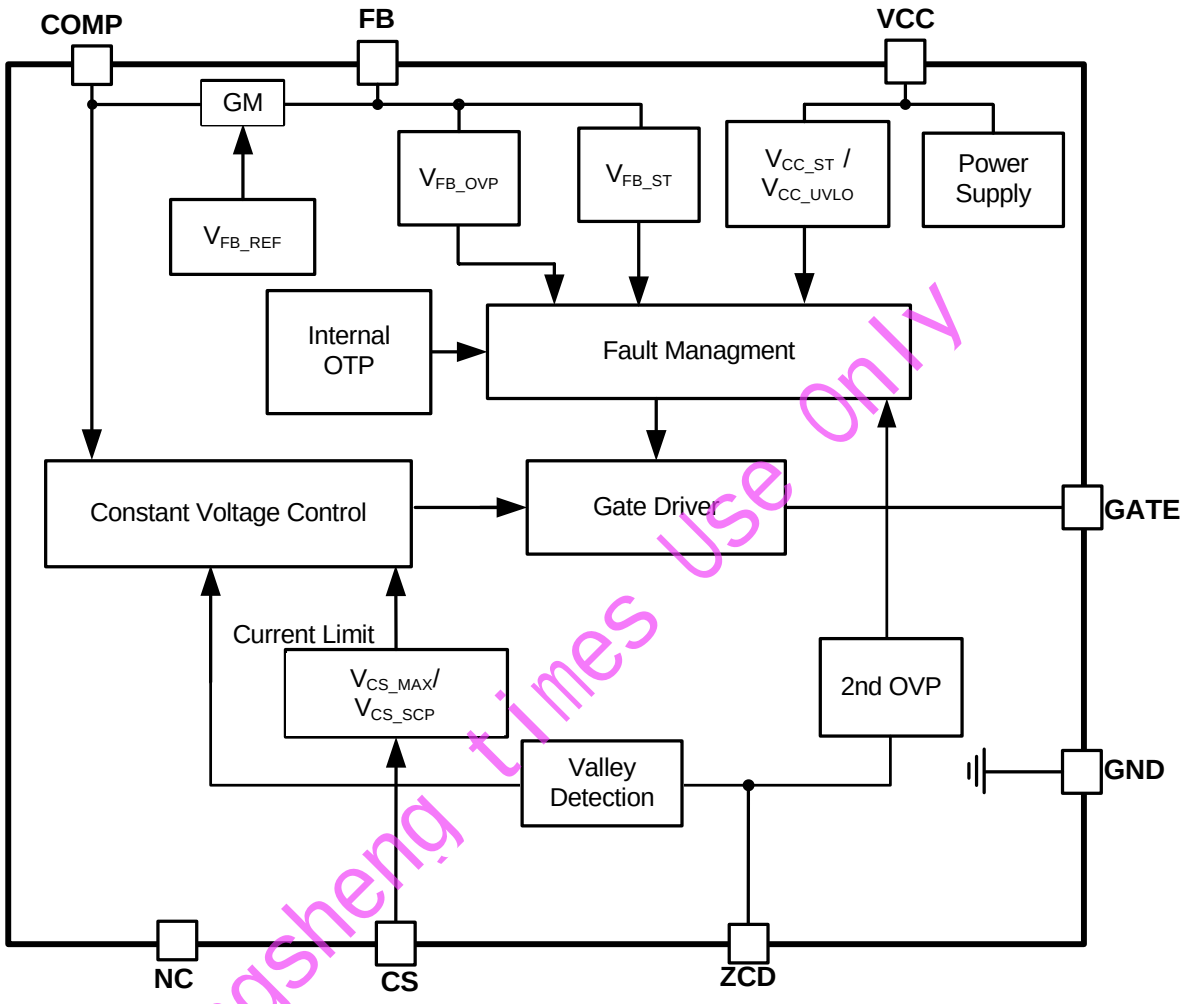
5) Guaranteed by design.

6) Derived from bench characterization. Not tested in production.

PIN FUNCTIONS

Pin SOP8	Name	Description
1	GATE	Gate driver for PFC MOSFET.
2	GND	Chip ground.
3	CS	Current sensing pin.
4	VCC	Power supply of IC.
5	FB	Output voltage feedback pin.
6	NC	
7	COMP	The error amplifier output is available on this pin. The network connected between this pin.
8	ZCD	Input from auxiliary winding for demagnetization timing and valley detection for PFC.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW1572 is a constant voltage (CV) controller which applies to non-isolation boost system with PFC. JW1572 can achieve excellent line and load regulation, high efficiency and low system cost with few peripheral components.

1. Start-up

When VCC is charged to VCC start-up voltage(V_{CC_ST})，GATE driver begins to switch. When VCC is lower than VCC under voltage lockout (V_{CC_UVLO}), IC stops switching.

2. Constant Voltage Control

JW1572 controls the output voltage by the information of FB pin. The output voltage is

$$V_{OUT} = \frac{V_{FB\_REF} \cdot (R_{FB1} + R_{FB2})}{R_{FB2}}$$

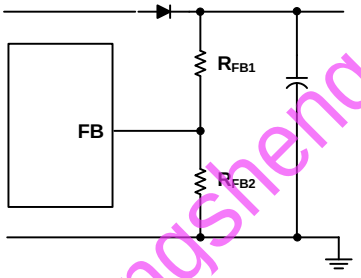


Figure.1 Output Sense

Where

V_{FB_REF}– FB Reference Voltage;

R_{FB1}, R_{FB2}– FB divide resistors.

3. Critical Conduction Mode Operation

JW1572 works in the critical conduction mode of the inductor current. When the power MOSFET is turned on, the inductor current increases from zero. Turn-on time of the MOSFET can be calculated as:

$$T_{ON} = \frac{I_{PK} \cdot L}{V_{IN}}$$

Where,

L– Inductance.

V_{IN}– Input voltage.

I_{PK} is the peak current in one switch period and the maximum value (I_{PK_MAX}) is limited by the MOSFET current sensing resistor (R_{CS}).

$$I_{PK\_MAX} = \frac{V_{CS\_MAX}}{R_{CS}}$$

V_{CS_MAX}– CS Cycle by Cycle limit Voltage.

When the power MOSFET is turned off, the inductor current begins to decrease. The power MOSFET turns on again when the inductor current is zero. Turn-off time of the MOSFET can be calculated as:

$$T_{OFF} = \frac{I_{PK} \cdot L}{V_{OUT} - V_{IN}}$$

Where,

V_{OUT} – output voltage.

The power inductance can be calculated as:

$$L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{f \cdot I_{PK} \cdot V_{OUT}}$$

Where, f is the frequency of the boost system.

4. Frequency Foldback

The maximum switching frequency is limited to F_{MAX}. At light load, switching frequency would fold back to F_{MIN}.

If the load further decreases, IC will enter the skip mode to minimize standby loss. Skip mode is realized by FB OVP.

5. Ipeak Enable Function

JW1572 enters I_{peak} enable mode when V_{FB} is lower than FB I_{peak} start-up Voltage ($V_{FB\_PK\_ST}$). Peak current is set as I_{PK_MAX}, which enhances heavy load dynamic response. JW1572 quits this mode when V_{FB} is higher than $V_{FB\_PK\_STOP}$.

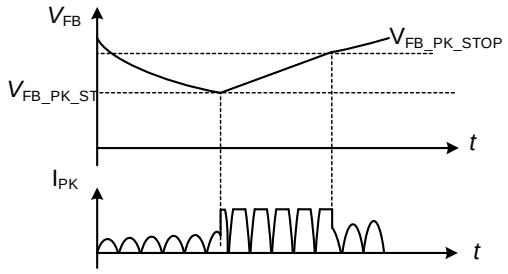


Figure.2 Ipeak Enable

6. Protection

JW1572 has multi-protection functions which largely enhance the safety and reliability of the system, including VCC UVLO, CS short current protection (SCP), FB over voltage protection, 2nd OVP and over temperature protection.

6.1 FB Over Voltage Protection

FB over voltage protection (OVP) is triggered if V_{FB} is higher than FB over voltage protection threshold (V_{FB_OVP}). The MOSFET gate driver stops unless FB voltage is decreased to V_{FB_OVP}-$V_{FB\_OVP\_HYST}$.

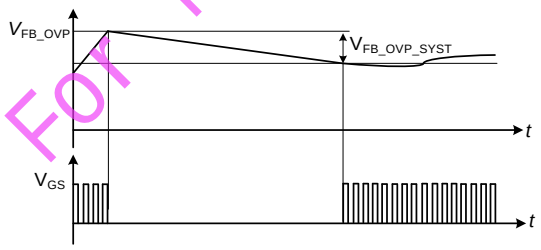


Figure.3 FB OVP

6.2 2nd OVP

The input voltage V_{IN} is detected by the sink current of ZCD pin during the main MOSFET on period, and the difference between output voltage V_{OUT} and input voltage V_{IN} can be detected by the source current of ZCD pin during the main MOSFET off period.

$$I_{SINK} = \frac{V_{IN} \cdot N_{aux}}{R_{ZCD} \cdot N_1}$$

$$I_{SOURCE} = \frac{(V_{OUT} - V_{IN}) \cdot N_{aux}}{R_{ZCD} \cdot N_1}$$

The output voltage V_{OUT} can be calculated by the threshold I_{OVP2}.

$$I_{OVP2} = |I_{SINK}| + |I_{SOURCE}|$$

$$V_{OVP2} = \frac{I_{OVP2} \cdot R_{ZCD} \cdot N_1}{N_{aux}}$$

If the output voltage sample signal exceeds I_{OVP2} for 3 consecutive switching cycles, 2nd OVP fault is asserted, and then the device shuts down, and restart after T_{FRD}.

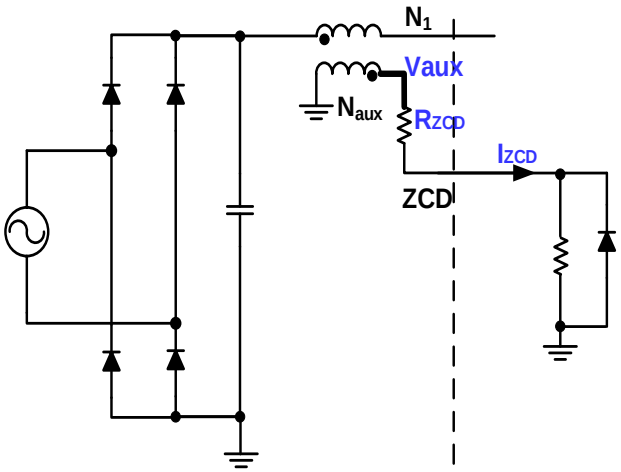


Figure.4 ZCD and Valley Detection

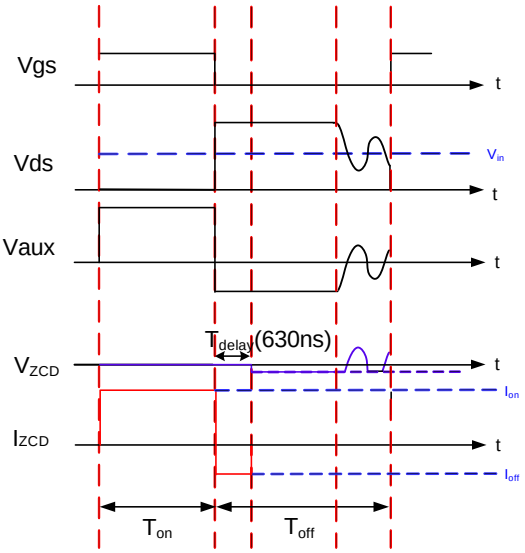


Figure.5 ZCD pin Current Sense Waveform

6.3 Disable Function

The FB pin can also be used for device disabling. If V_{FB} is pulled down and lower than FB start-up voltage (V_{FB_ST}), JW1572 stops switching and enters in green mode which reduces the power consumption. JW1572 will restart if $V_{FB}>V_{FB\_ST}$.

6.4 Over Temperature Protection

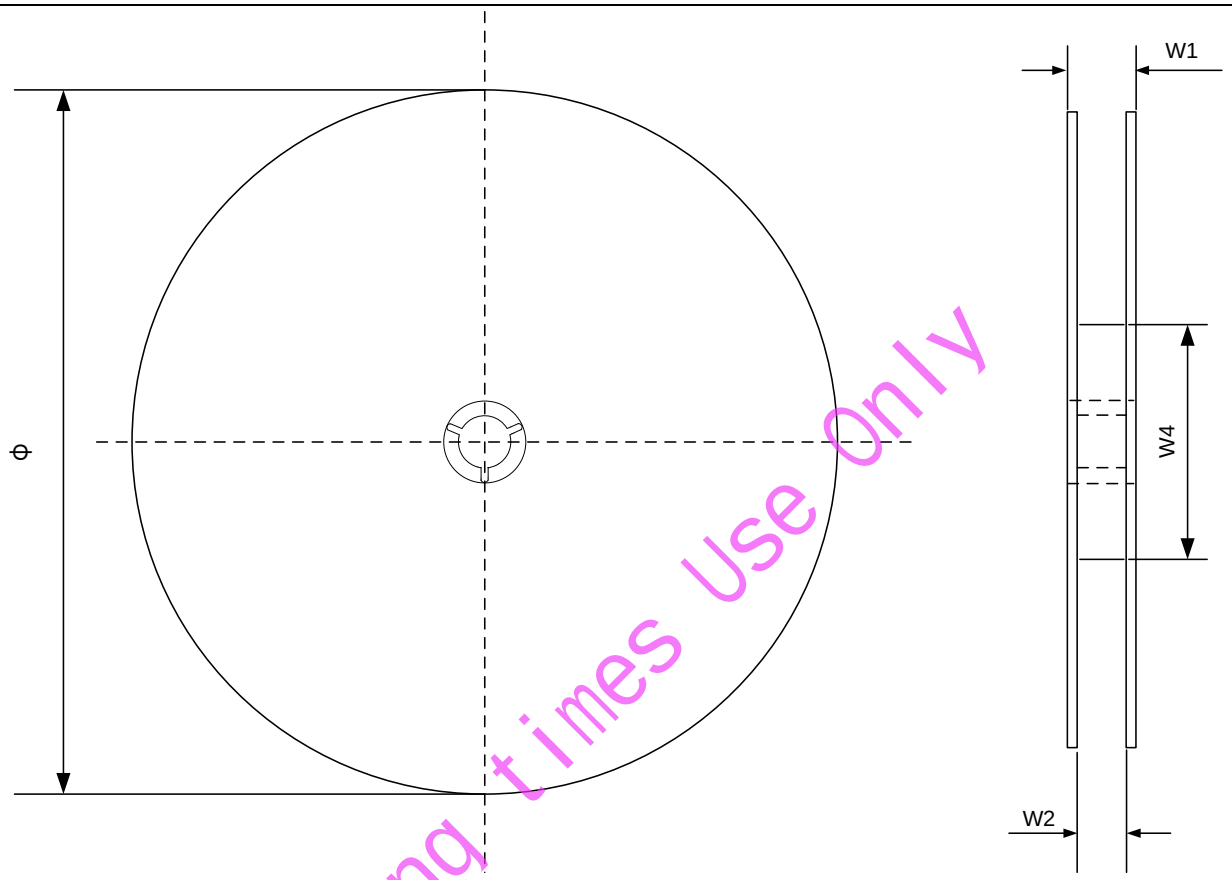
JW1572 provides internal over thermal protection. When internal temperature of IC exceeds the inner over thermal protection threshold (T_{OTP}), JW1572 stops switching unless the junction temperature decreases to T_{OTP}-T_{OTP_HYST}.

6.5 Short Current Protection

If V_{CS} exceeds V_{CS_SCP} within T_{LEB1}, the switch will be turned off right now and restart after T_{FRD}. This causes the SCP fault.

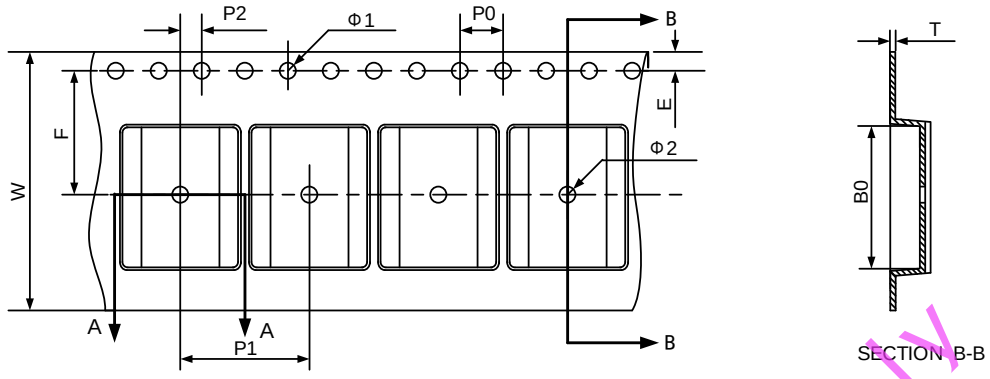
TAPE AND REEL INFORMATION

Reel UNIT: mm

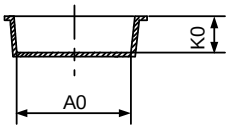


Package	Diameter Φ	Thickness W1	Width W2	W4
SOP8	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm



SECTION B-B



SECTION A-A

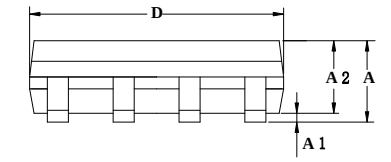
Note :

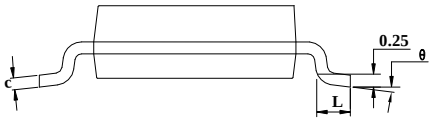
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

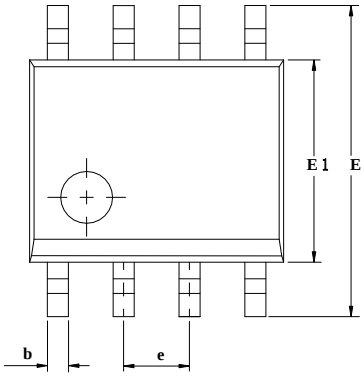
Package	Tape dimensions(mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
SOP8	4.0±0.1	2.0±0.1	8.0±0.1	6.40±0.3	5.35±0.3	12.0±0.3	0.25±0.2	2.00±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10

PACKAGE OUTLINE

SOP8 UNIT: mm

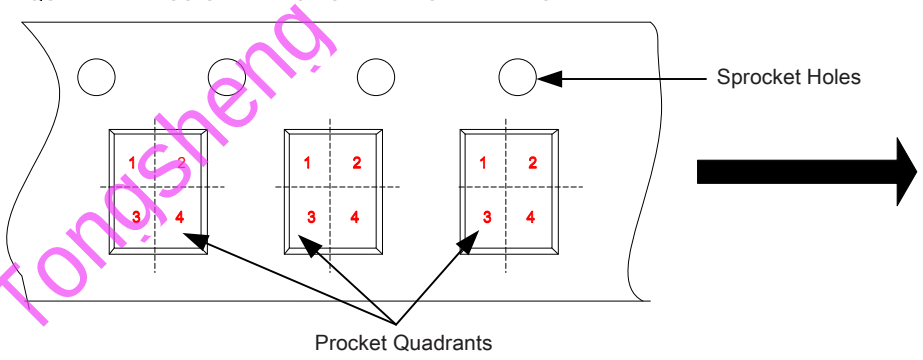






Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOP8	1

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