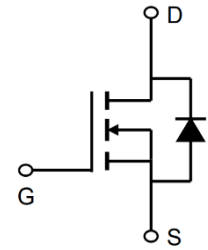


## 85V N-Channel Enhancement Mode MOSFET

### Description

The AP90N08NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V.

This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 85V$   $I_D = 95A$

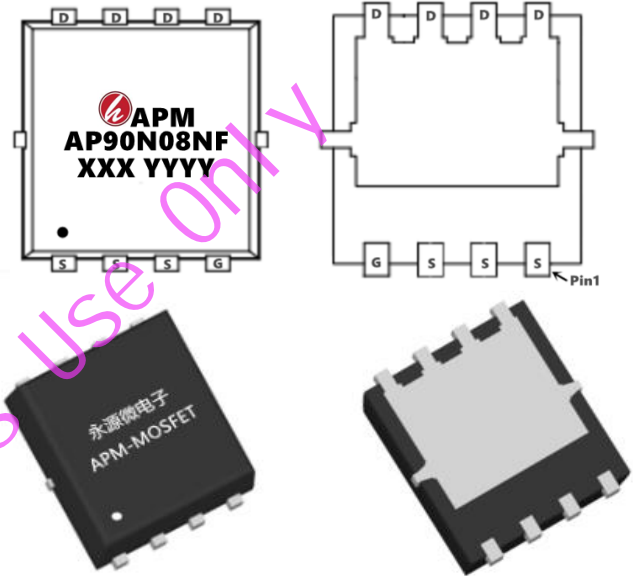
$R_{DS(ON)} < 5.2m\Omega$   $V_{GS}=10V$  (Type: 4.5m $\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP90N08NF	PDFN5*6-8L	AP90N08NF XXX YYYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	85	V
VGS	Gate-Source Voltage	$\pm 20$	V
$I_{D@TC=25^\circ C}$	Continuous Drain Current, VGS @ 10V	95	A
$I_{D@TC=100^\circ C}$	Continuous Drain Current, VGS @ 10V	75	A
IDM	Pulsed Drain Current	480	A
EAS	Single Pulse Avalanche Energy	560	mJ
IAS	Avalanche Current	43.4	A
$PD@TC=25^\circ C$	Total Power Dissipation <sup>4</sup>	180	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
TJ	Operating Junction Temperature Range	-55 to 150	$^\circ C$
R $\theta$ JA	Thermal Resistance Junction-Ambient	0.70	$^\circ C/W$
R $\theta$ JC	Thermal Resistance Junction-Case	62	$^\circ C/W$



## 85V N-Channel Enhancement Mode MOSFET

### Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	80	92		V
VGS(th)	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A, T_J=25^\circ\text{C}$	2.0	3.0	4.0	V
IDSS	Zero gate voltage drain current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	-		1	$\mu A$
IDSS	Zero gate voltage drain current	$V_{DS}=80V, V_{GS}=0V, T_J=125^\circ\text{C}$		- 5		$\mu A$
IGSS	Gate-source leakage current	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
RDS(on)	Drain-source on-state resistance	$V_{GS}=10V, I_D=50A, T_J=25^\circ\text{C}$	-	4.5	5.2	m $\Omega$
gfs	Transconductance	$V_{DS}=5V, I_D=50A$	-	80	-	S
Ciss	Input Capacitance	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$	-	4032	-	pF
Coss	Output Capacitance		-	546	-	pF
Crss	Reverse Transfer Capacitance	$V_{GS}=10V, V_{DS}=40V, I_D=25A$	-	35	-	pF
Q <sub>G</sub>	Gate Total Charge		-	65.7	-	nC
Q <sub>gs</sub>	Gate-Source charge		-	24.9	-	nC
Q <sub>gd</sub>	Gate-Drain charge		-	13.9	-	nC
td(on)	Turn-on delay time	$T_J=25^\circ\text{C}, V_{GS}=10V, V_{DS}=40V, R_L=3\Omega$	-	20.1	-	ns
t <sub>r</sub>	Rise time		-	38	-	ns
td(off)	Turn-off delay time		-	45.1	-	ns
t <sub>f</sub>	Fall time		-	21	-	ns
R <sub>G</sub>	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1\text{MHz}$	-	2	-	$\Omega$
VSD	Body Diode Forward Voltage	$V_{GS}=0V, I_{SD}=50A$	-	0.9	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=20A, dI/dt=500A/\mu s$	-	61	-	ns
Qrr	Body Diode Reverse Recovery Charge	$I_F=20A, dI/dt=500A/\mu s$	-	340	-	nC

#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、 The test cond  $\cong 300\mu s$  duty cycle  $\cong 2\%$ , duty cycle ition is  $V_{DD}=64V_{GS}=10V, L=0.1mH, I_{AS}=53.8A$
- 4、 The power dissipation is limited by 175 $^\circ\text{C}$  junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

### Typical Characteristics

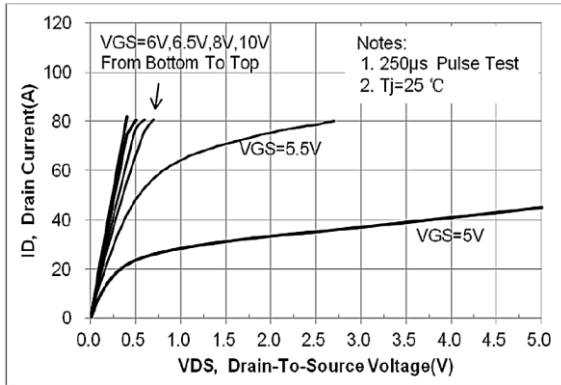


Figure 1. Typ. Output Characteristics (Tj=25 °C)

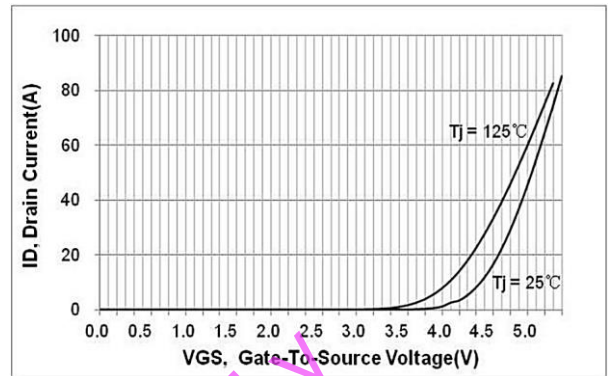


Figure 2. Transfer Characteristics

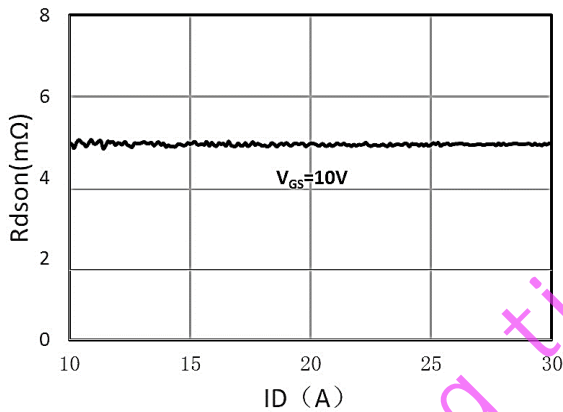


Figure 3. On-Resistance vs. Drain Current and Gate Voltage Figure

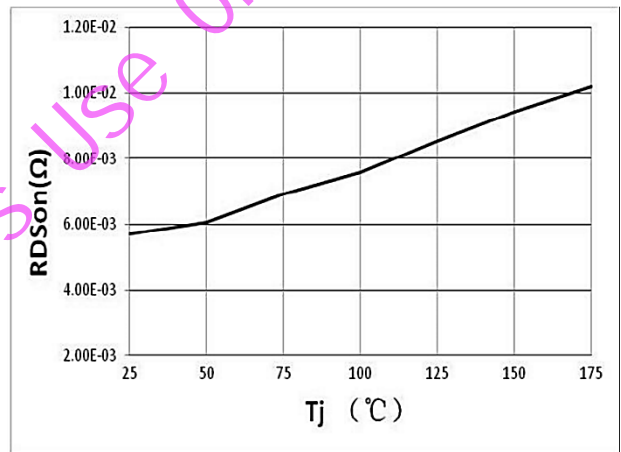


Figure 4. On-Resistance vs. Junction Temperature

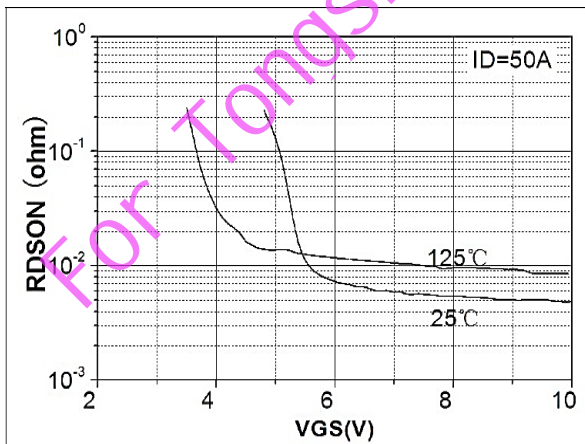


Figure 5. On-Resistance vs. Gate-Source Voltage

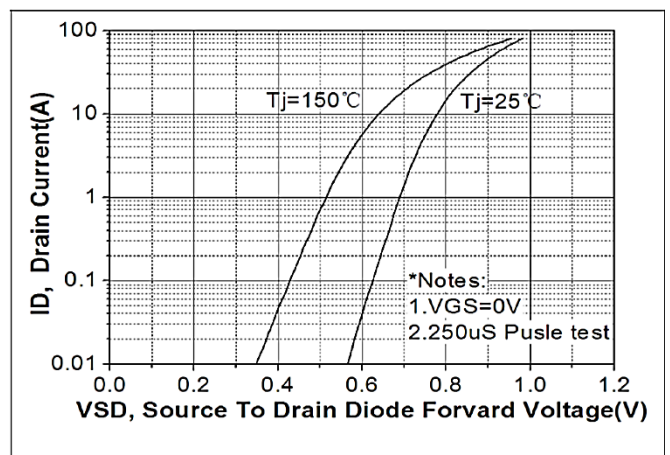


Figure 6 . Body-Diode Characteristics

## 85V N-Channel Enhancement Mode MOSFET

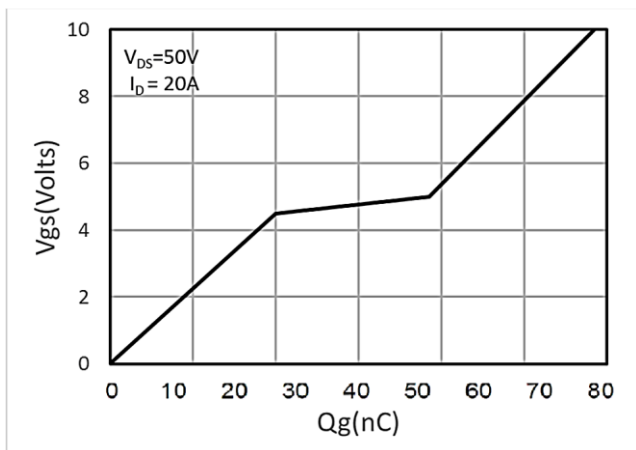


Figure 7. Gate-Charge Characteristics

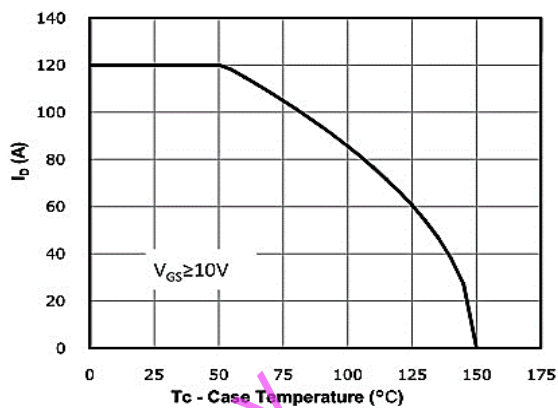


Figure 8. Drain Current Derating

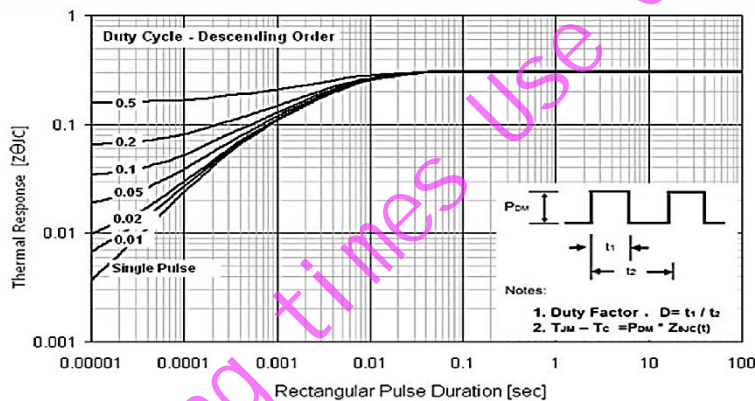


Figure 9: Normalized Maximum Transient Thermal Impedance

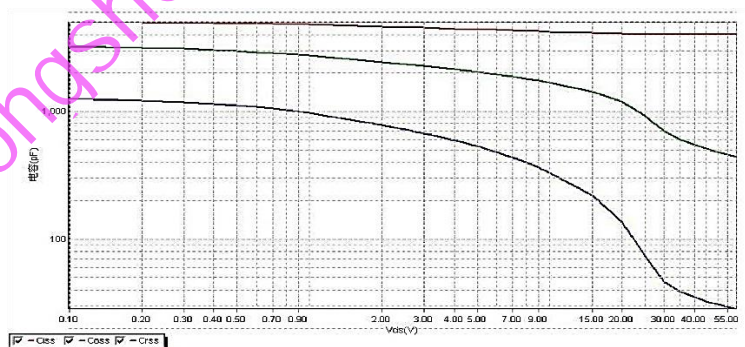
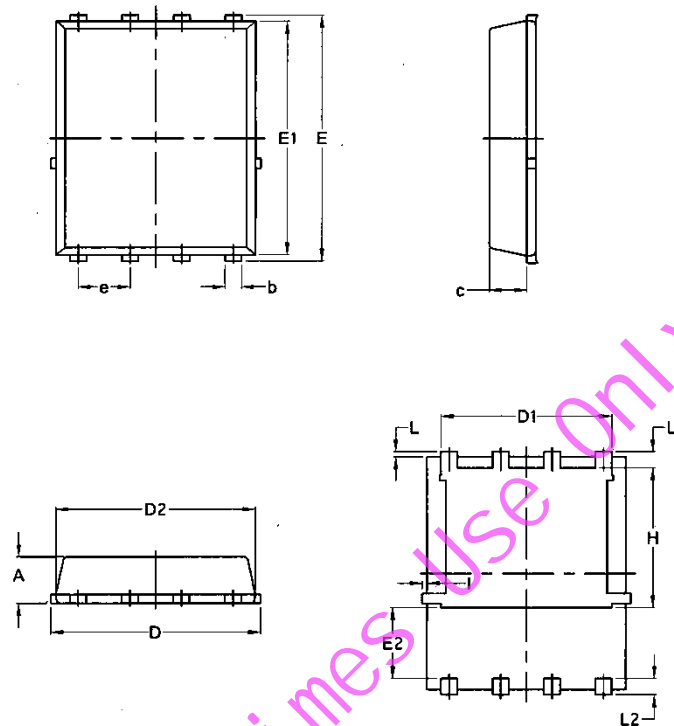


Figure 10. Capacitance Characteristics

### Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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## 85V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/12/1	Initial release

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