

## 40V N+P-Channel Enhancement Mode MOSFET

### Description

The AP6G04S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 6.3A$

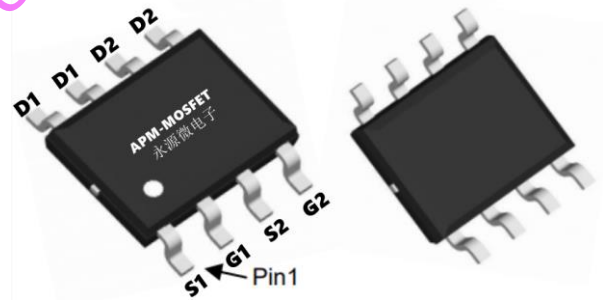
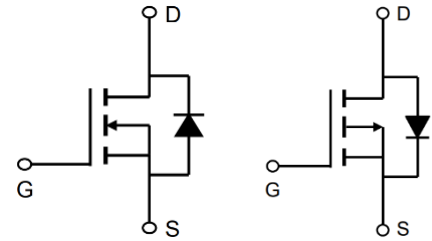
$R_{DS(ON)} < 37m\Omega$  @  $V_{GS}=10V$  (Type: 30m $\Omega$ )

$V_{DS} = -40V$   $I_D = -6.1A$

$R_{DS(ON)} < 75m\Omega$  @  $V_{GS}=-10V$  (Type: 62m $\Omega$ )

### Application

- Wireless charging
- Boost driver
- Brushless motor



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP6G04S	SOP-8	AP6G04S XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
$V_{DS}$	Drain-Source Voltage	40	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.3	-6.1	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.9	-4.8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	23	-22	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	16.2	39	mJ
$I_{AS}$	Avalanche Current	6.8	-6.8	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	1.67	1.67	W
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	75		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	30		$^\circ C/W$

**40V N+P-Channel Enhancement Mode MOSFET****N-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	44	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.032	---	$V/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=4A$	---	30	37	m $\Omega$
		$V_{GS}=4.5V, I_D=3A$	---	40	50	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.5	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu\text{A}$
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=4A$	---	8	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.4	4.8	$\Omega$
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	5	---	nC
Qgs	Gate-Source Charge		---	1.54	---	
Qgd	Gate-Drain Charge		---	1.84	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	---	7.8	---	ns
Tr	Rise Time		---	2.1	---	
Td(off)	Turn-Off Delay Time		---	29	---	
Tf	Fall Time		---	2.1	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	452	---	pF
Coss	Output Capacitance		---	51	---	
Crss	Reverse Transfer Capacitance		---	38	---	
IS	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	4.5	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	14	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

**40V N+P-Channel Enhancement Mode MOSFET****P-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-40	-44	---	V
ΔBVDSS/ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.018	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-3A	---	62	75	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2A	---	81	100	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	-1.5	-2.5	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	2.5	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3A	---	5.8	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-32V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	6.4	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.1	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =-20V, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-3A	---	4.2	---	ns
T <sub>r</sub>	Rise Time		---	23	---	
Td(off)	Turn-Off Delay Time		---	26.8	---	
T <sub>f</sub>	Fall Time		---	20.6	---	
Ciss	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	620	---	pF
Coss	Output Capacitance		---	65	---	
Crss	Reverse Transfer Capacitance		---	53	---	
IS	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-3.2	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	-16.1	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1	V

**Note :**

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≅ 300us, duty cycle ≅ 2%
3. The power dissipation is limited by 150°C junction temperature
4. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

### N-Typical Characteristics

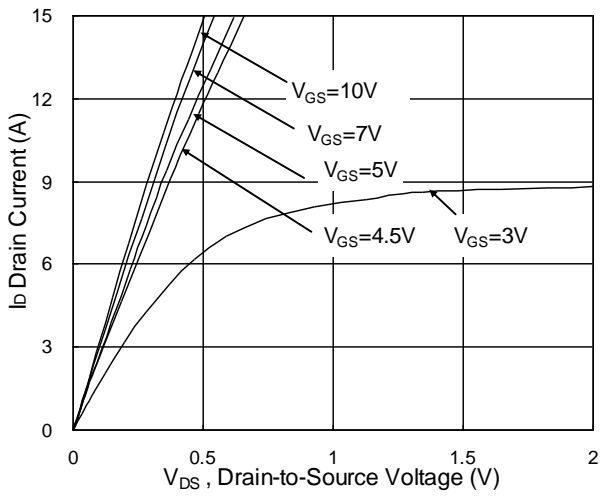


Fig.1 Typical Output Characteristics

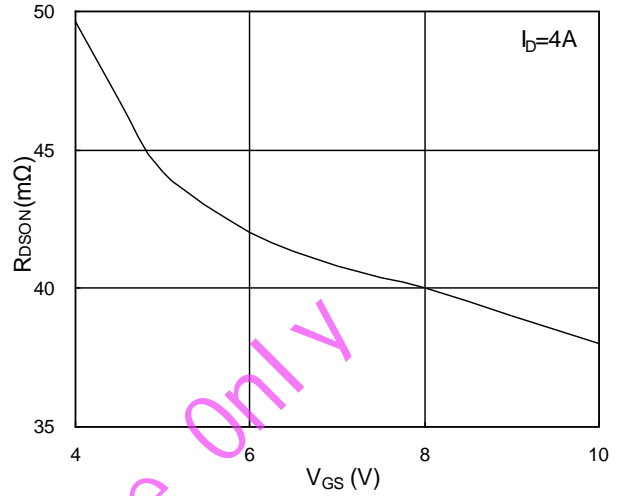


Fig.2 On-Resistance vs. Gate-Source

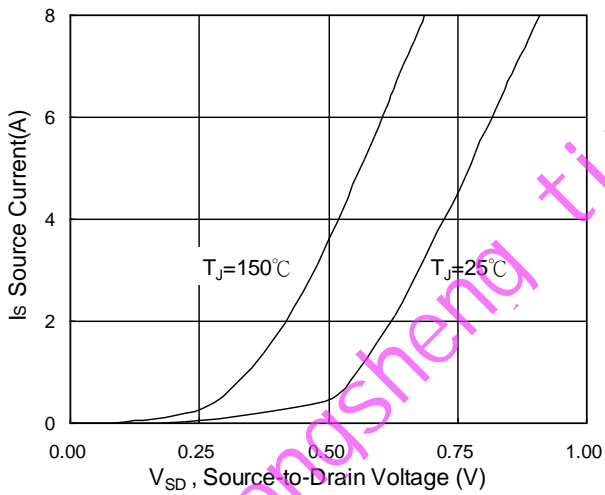


Fig.3 Forward Characteristics Of Reverse

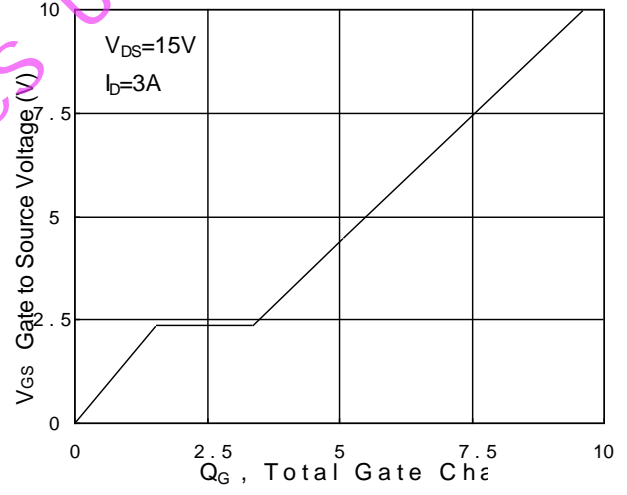


Fig.4 Gate-Charge Characteristics

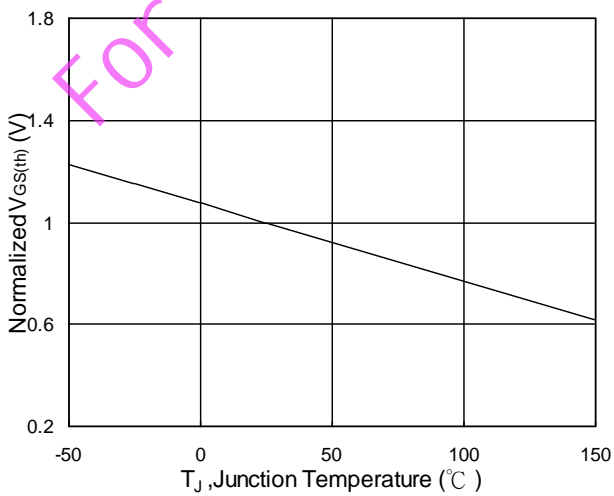


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

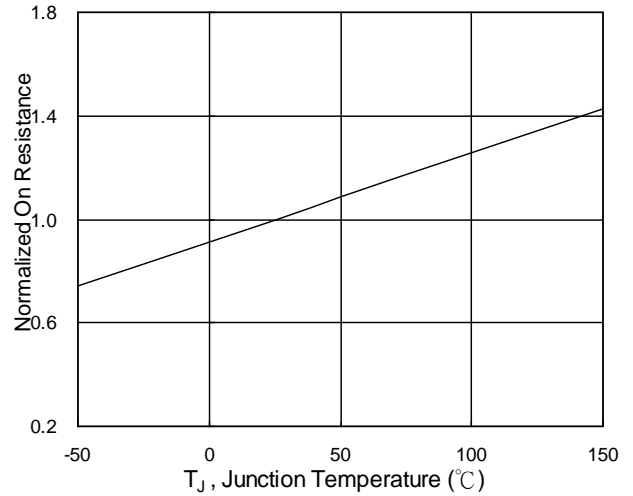
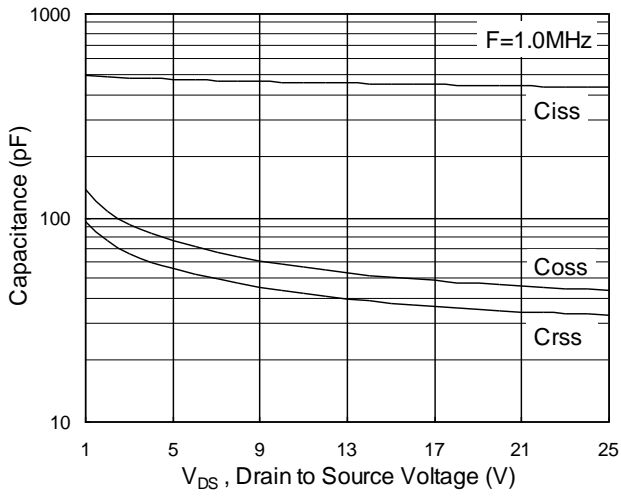
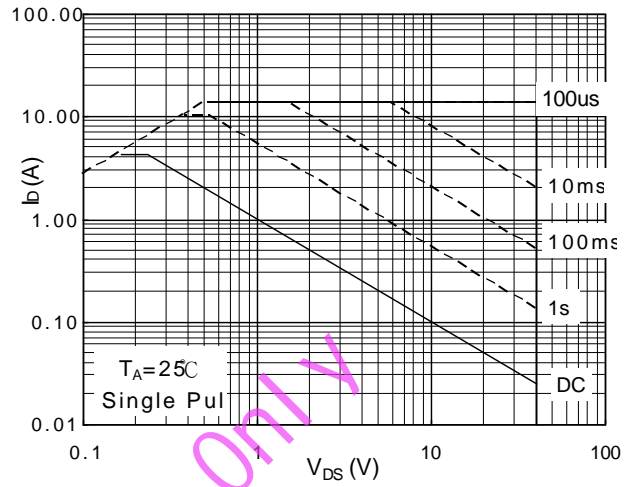


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

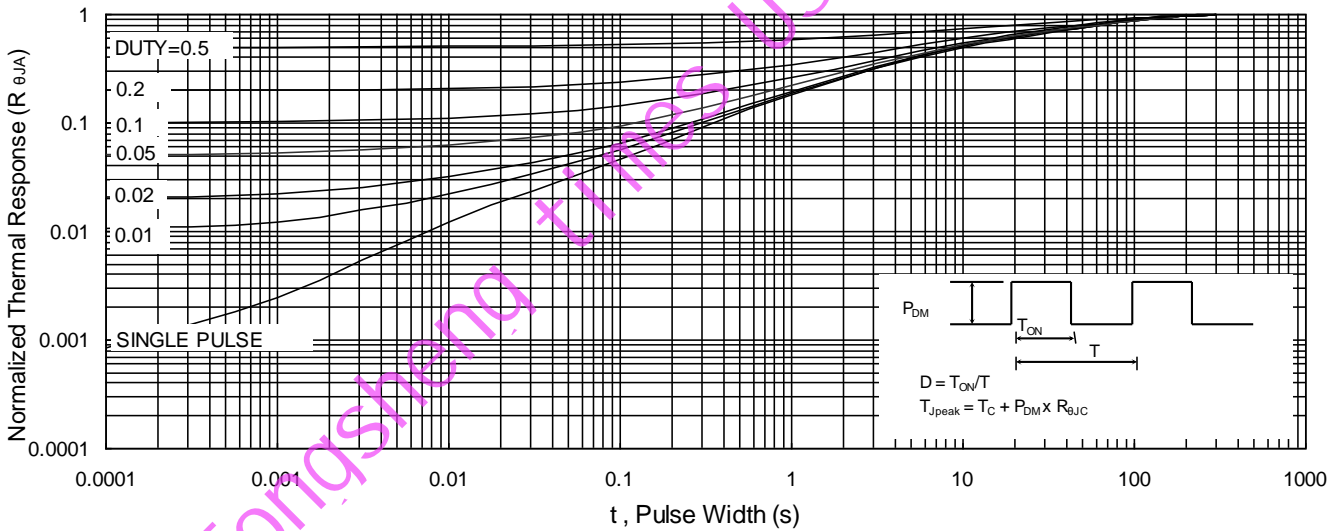
**40V N+P-Channel Enhancement Mode MOSFET**



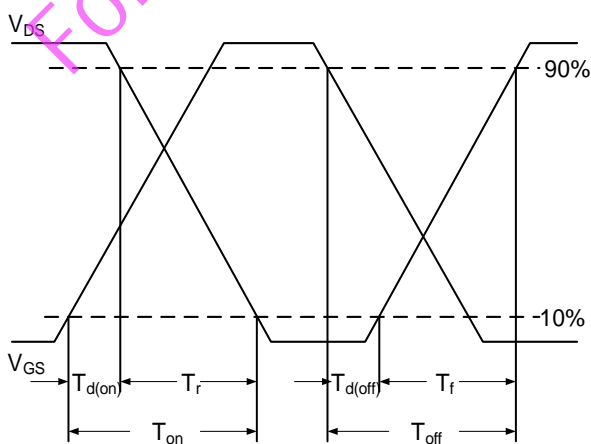
**Fig.7 Capacitance**



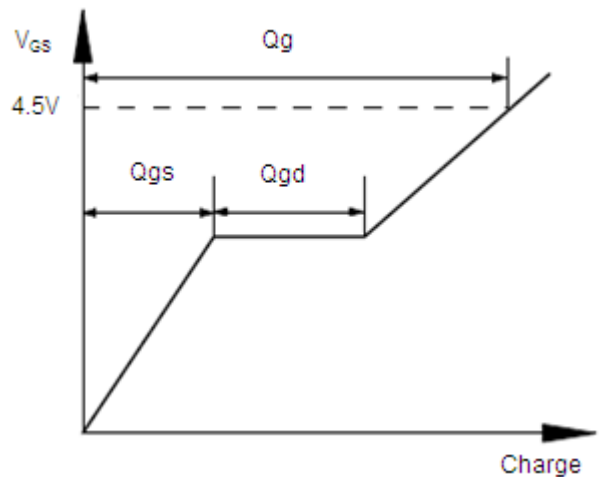
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

### P-Typical Characteristics

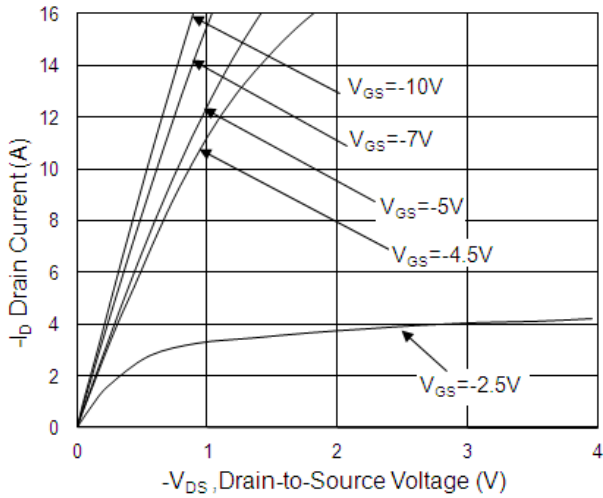


Fig.1 Typical Output Characteristics

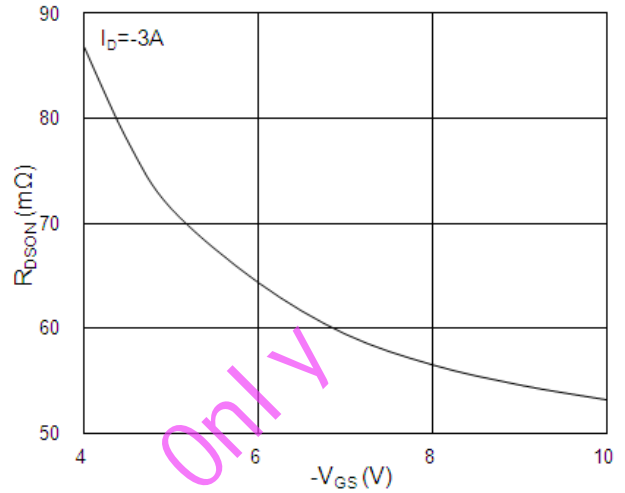


Fig.2 On-Resistance vs. G-S Voltage

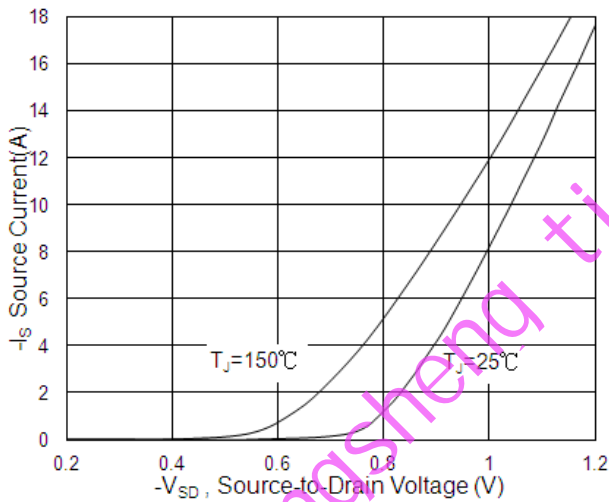


Fig.3 Forward Characteristics Of Reverse

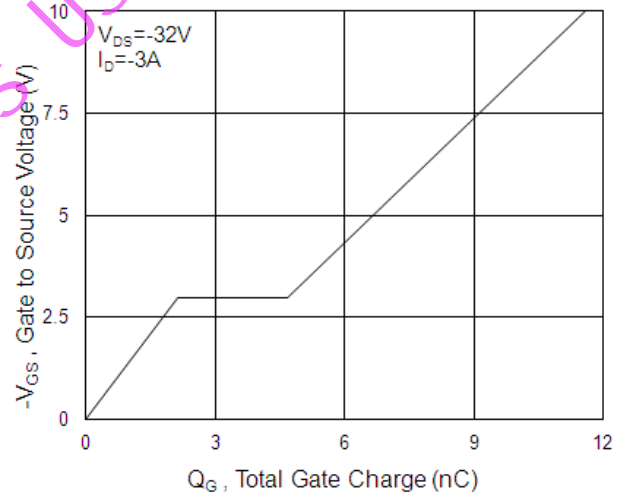


Fig.4 Gate-Charge Characteristics

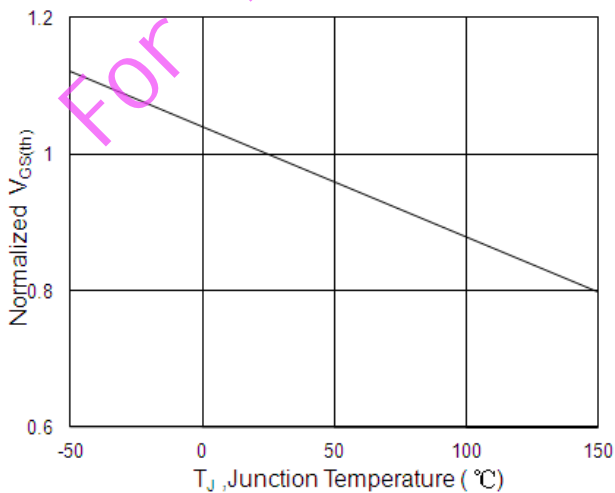


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

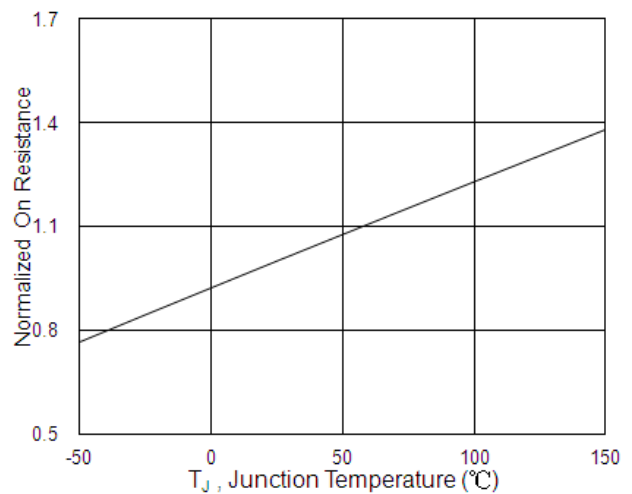


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

## 40V N+P-Channel Enhancement Mode MOSFET

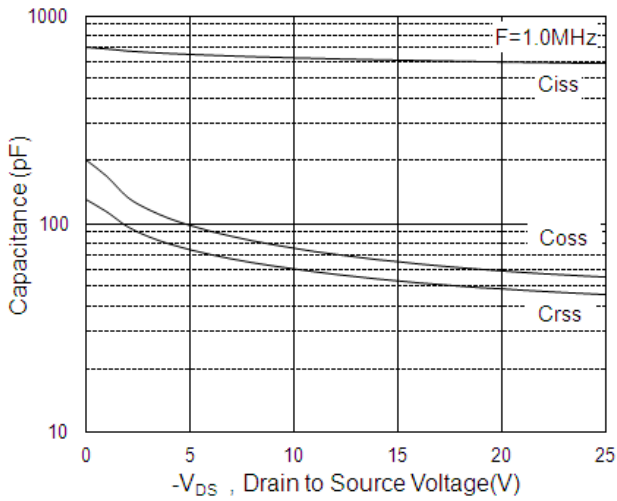


Fig.7 Capacitance

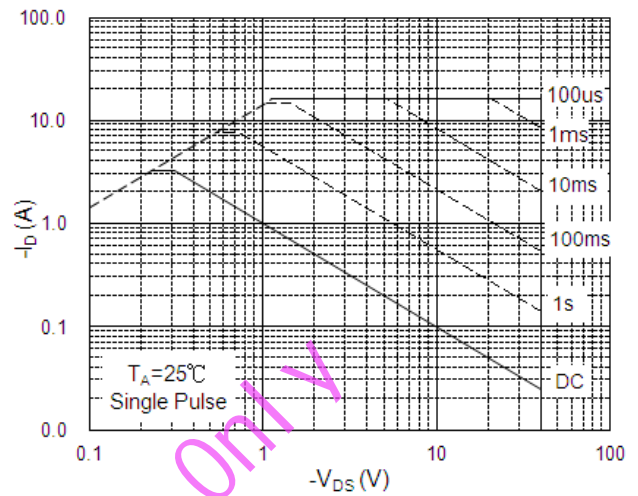


Fig.8 Safe Operating Area

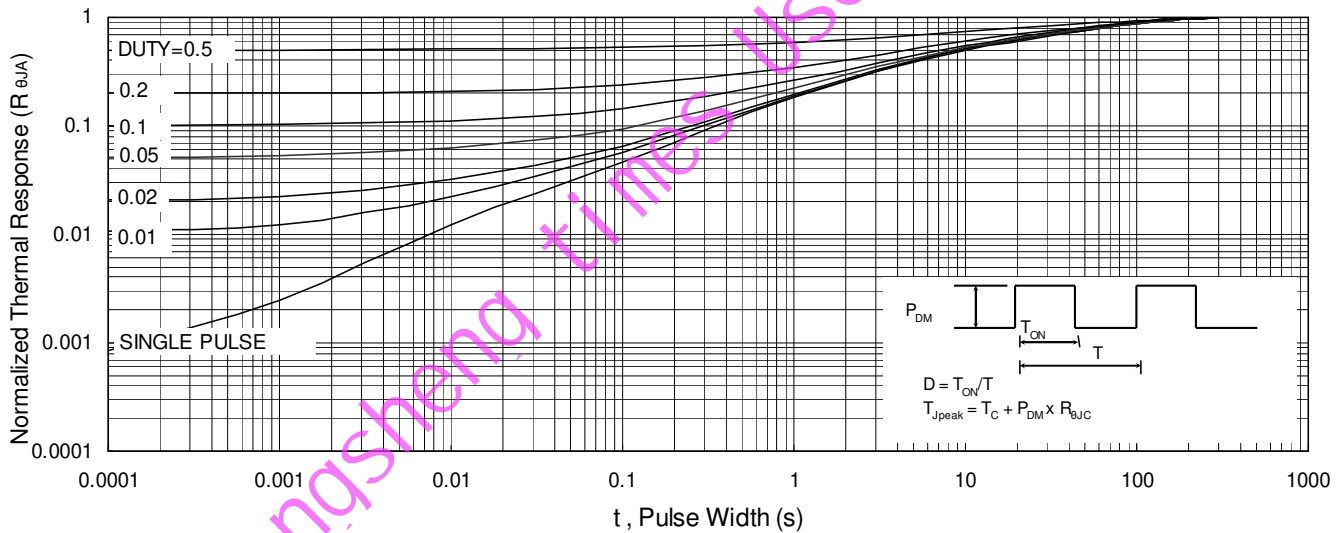


Fig.9 Normalized Maximum Transient Thermal Impedance

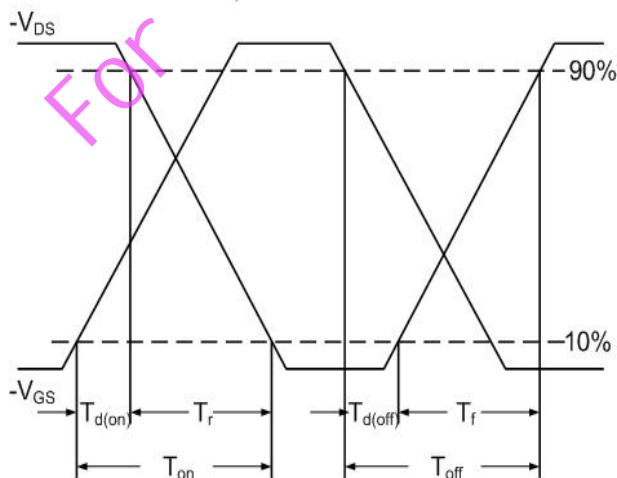


Fig.10 Switching Time Waveform

Data and specifications subject to change without notice.

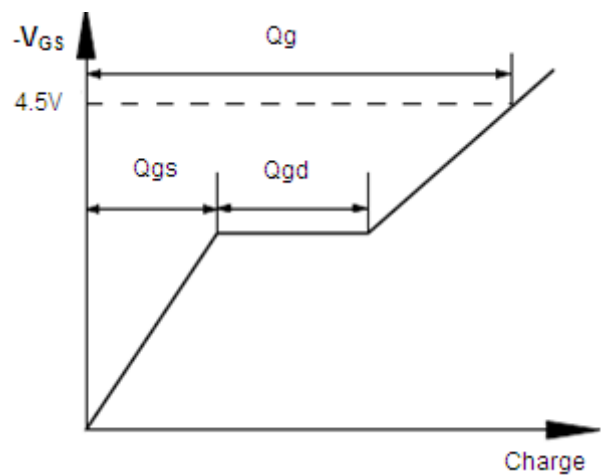
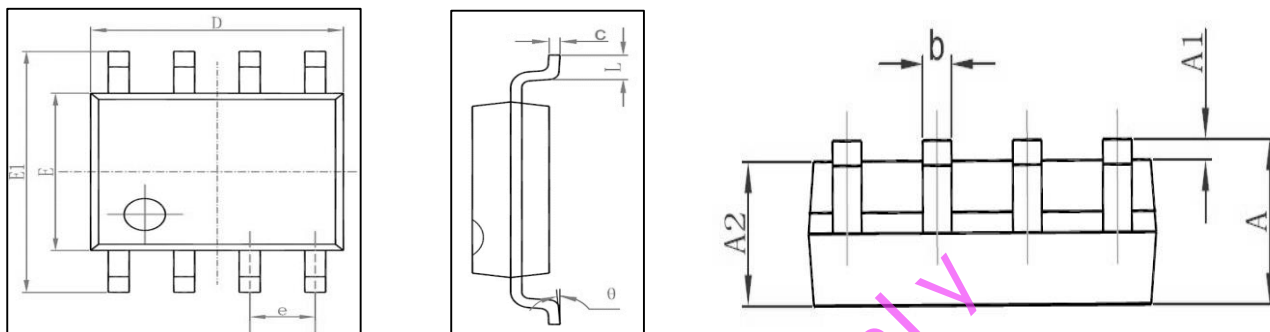


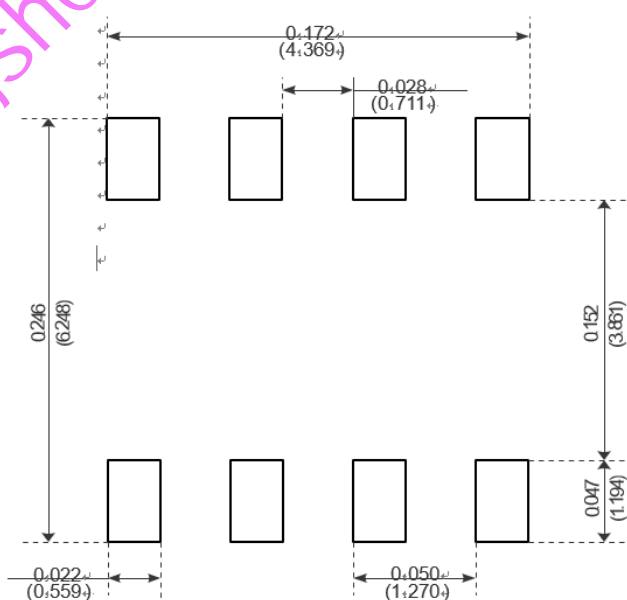
Fig.11 Gate Charge Waveform



### Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads



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# AP6G04S

## 40V N+P-Channel Enhancement Mode MOSFET

Edition	Date	Change
RVE1.0	2018/01/31	Initial release

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