

20V N-Channel Enhancement Mode MOSFET

Description

The NP2302D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and high density cell Design for ultra low on-resistance. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = 20V$, $I_D = 3A$
 $R_{DS(ON)}(Typ.) = 41m\Omega$ @ $V_{GS} = 2.5V$
 $R_{DS(ON)}(Typ.) = 31.3m\Omega$ @ $V_{GS} = 4.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

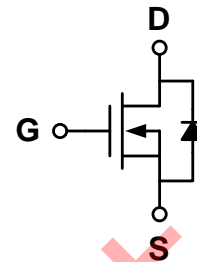
Application

- ◆ PWM applications
- ◆ Load switch

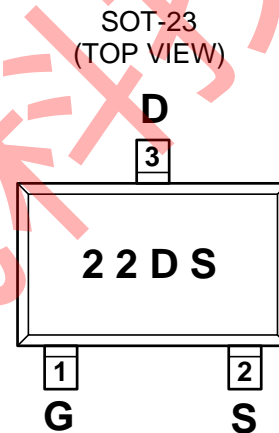
Package

- ◆ SOT-23

Schematic diagram



Marking and pin assignment



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP2302DVR	-55°C to +150°C	SOT-23	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	±12	V
Drain current-continuous ^a @Tj=125°C -pulse ^b	I_D	3	A
	I_{DM}	12	A
Drain-source Diode forward current	I_S	1.6	A
Maximum power dissipation	P_D	1.25	W
Operating junction Temperature range	T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.75	1.2	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=3A$	-	31.3	45	m Ω
		$V_{GS}=2.5V, I_D=2.8A$	-	41	65	
Forward transconductance	g_{fs}	$V_{GS}=5V, I_D=3A$	-	5	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=10V, V_{GS}=0V$ $f=1.0MHz$	-	240	-	pF
Output capacitance	C_{OSS}		-	45	-	
Reverse transfer capacitance	C_{RSS}		-	23	-	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	$V_{DD}=10V$ $R_L=3.3\ ohm$ $V_{GEN}=4.5V$ $R_{GEN}=60\ ohm$	-	2.3	-	ns
Rise time	t_r		-	3.1	-	
Turn-off delay time	$t_{D(OFF)}$		-	21	-	
Fall time	t_f		-	2.6	-	
Total gate charge	Q_g	$V_{DS}=10V$ $I_D=3A$ $V_{GS}=4.5V$	-	2.7	-	nC
Gate-source charge	Q_{gs}		-	0.4	-	
Gate-drain charge	Q_{gd}		-	0.5	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_S=3A$	-	0.76	1.16	V

Notes:

- surface mounted on FR4 board, $t \leq 10sec$
- pulse test: pulse width $\leq 300\mu s$, duty $\leq 2\%$
- guaranteed by design, not subject to production testing

Thermal Characteristics

Thermal Resistance junction-to ambient	Rth JA	100	$^{\circ}C/W$
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Typical Performance Characteristics

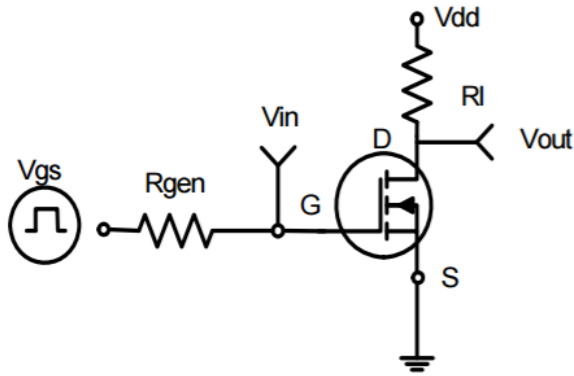


Figure 1: Switching Test Circuit

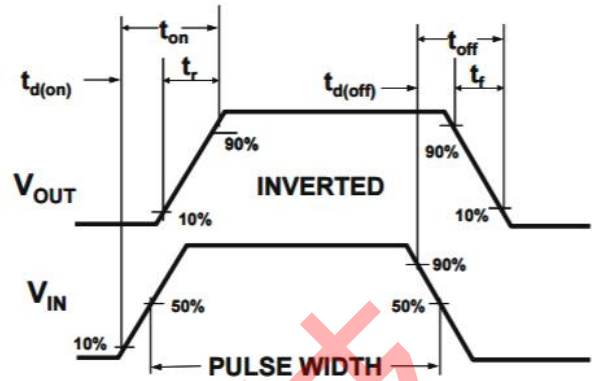


Figure 2: Switching Waveforms

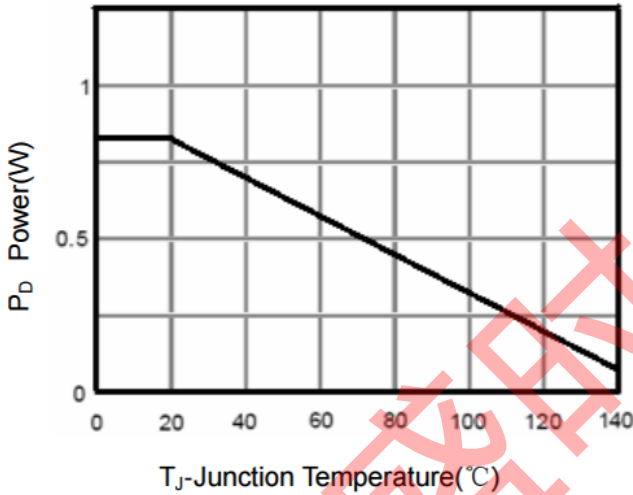


Figure 3 Power Dissipation

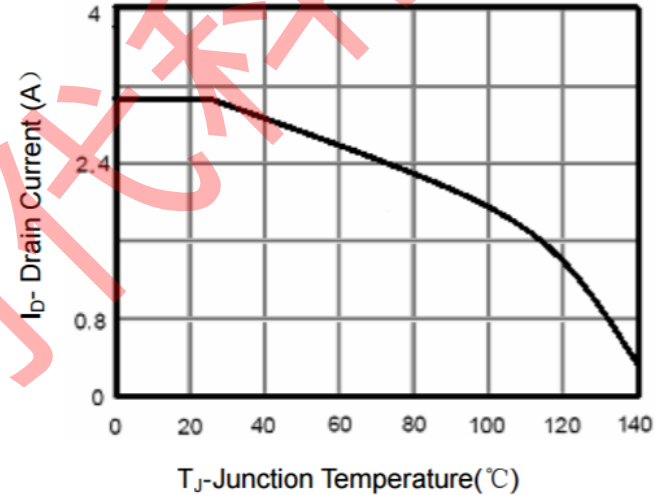


Figure 4 Drain Current

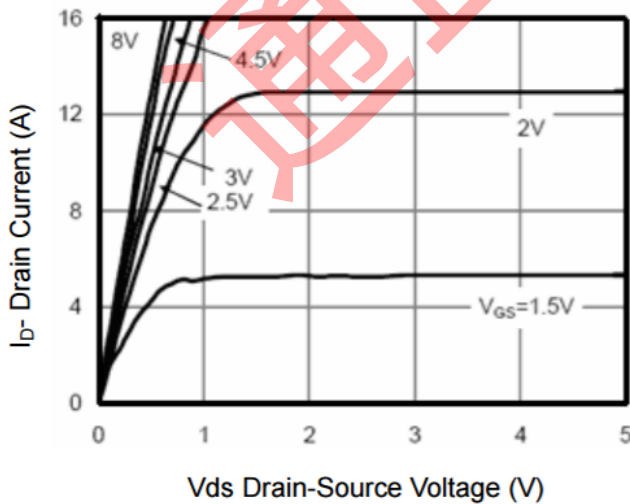


Figure 5 Output Characteristics

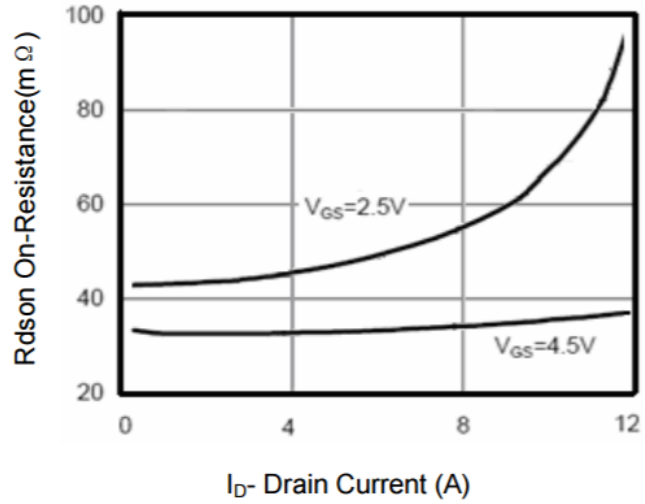


Figure 6 Drain-Source On-Resistance

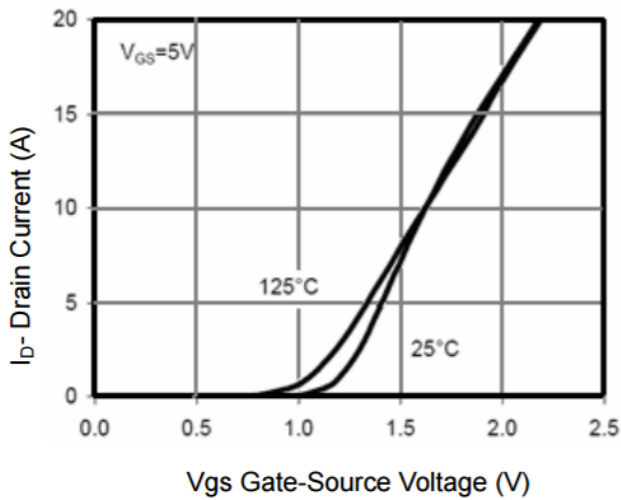


Figure 7 Transfer Characteristics

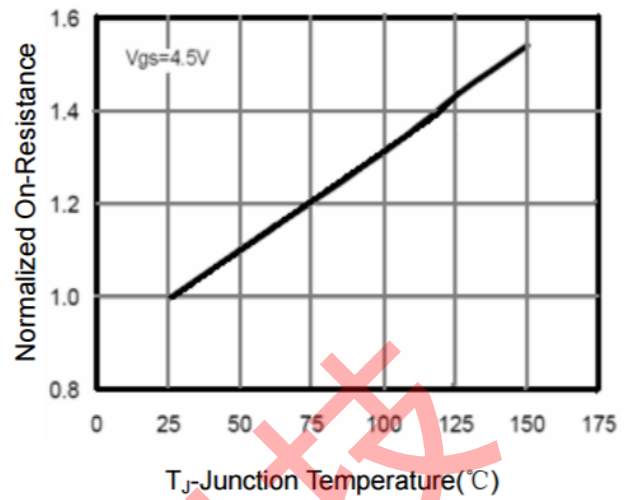


Figure 8 Drain-Source On-Resistance

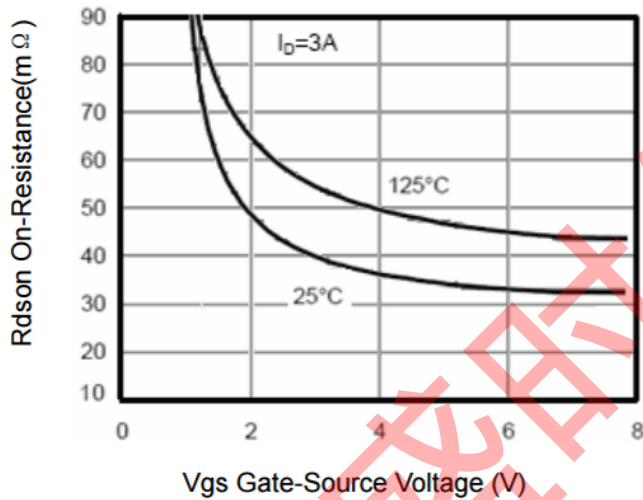


Figure 9 Rds(on) vs Vgs

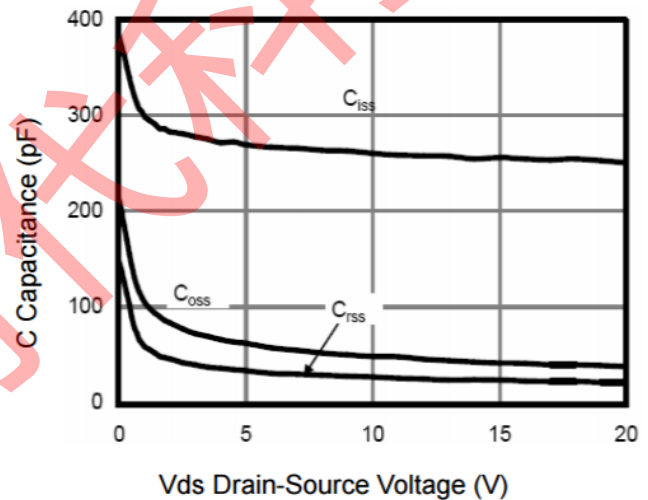


Figure 10 Capacitance vs Vds

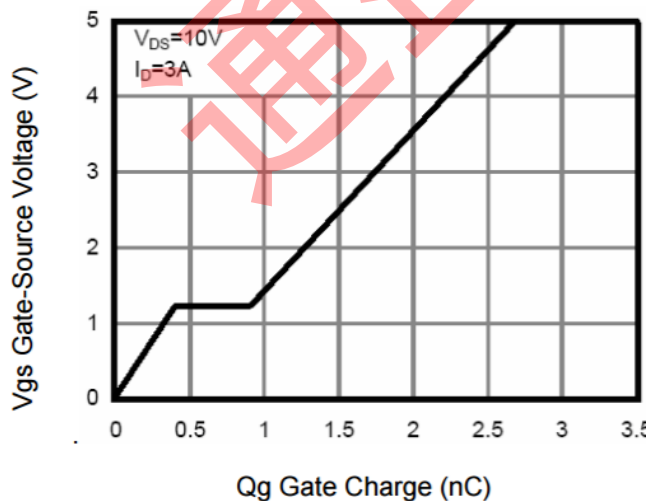


Figure 11 Gate Charge

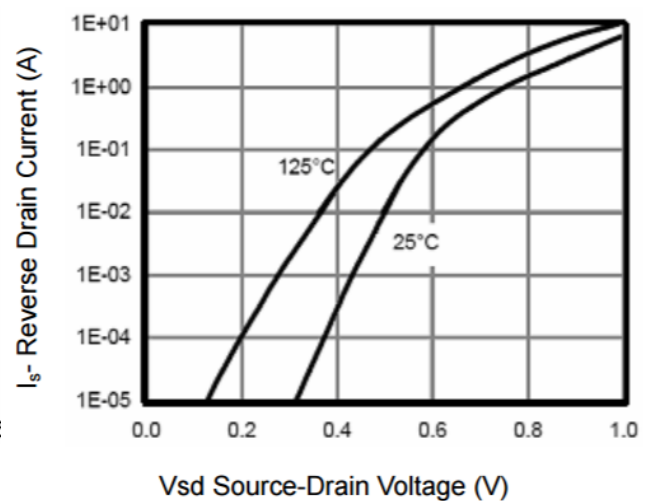


Figure 12 Source- Drain Diode Forward

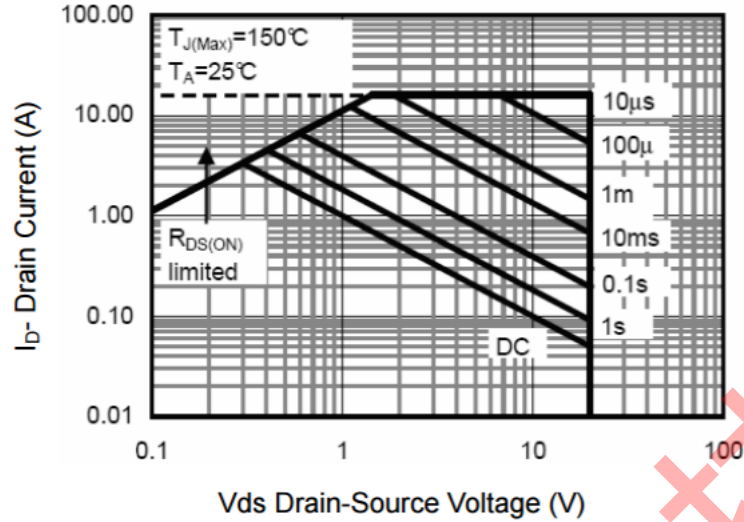


Figure 13 Safe Operation Area

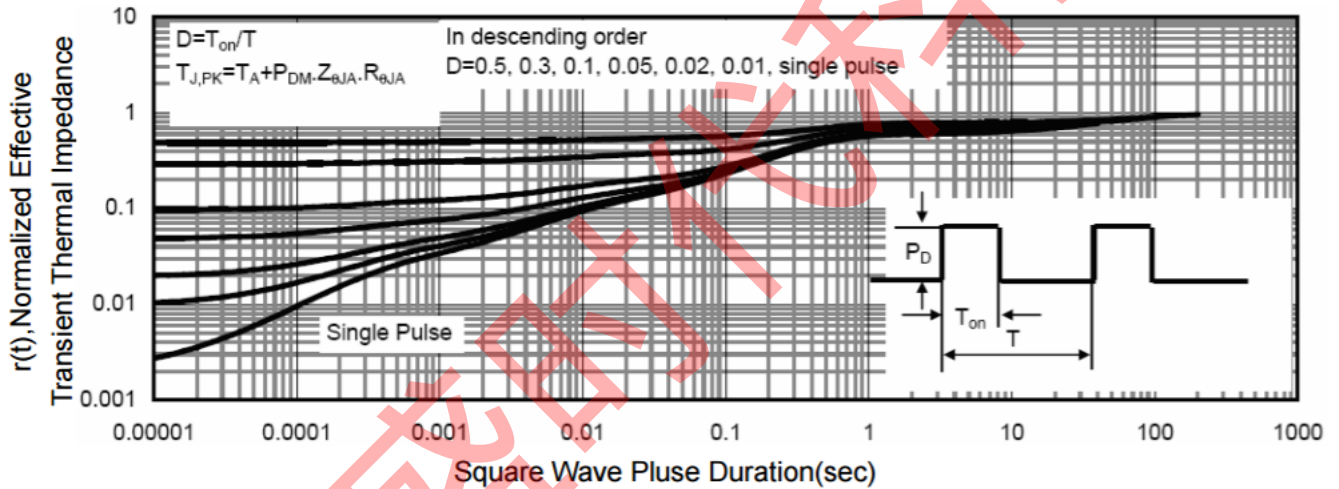
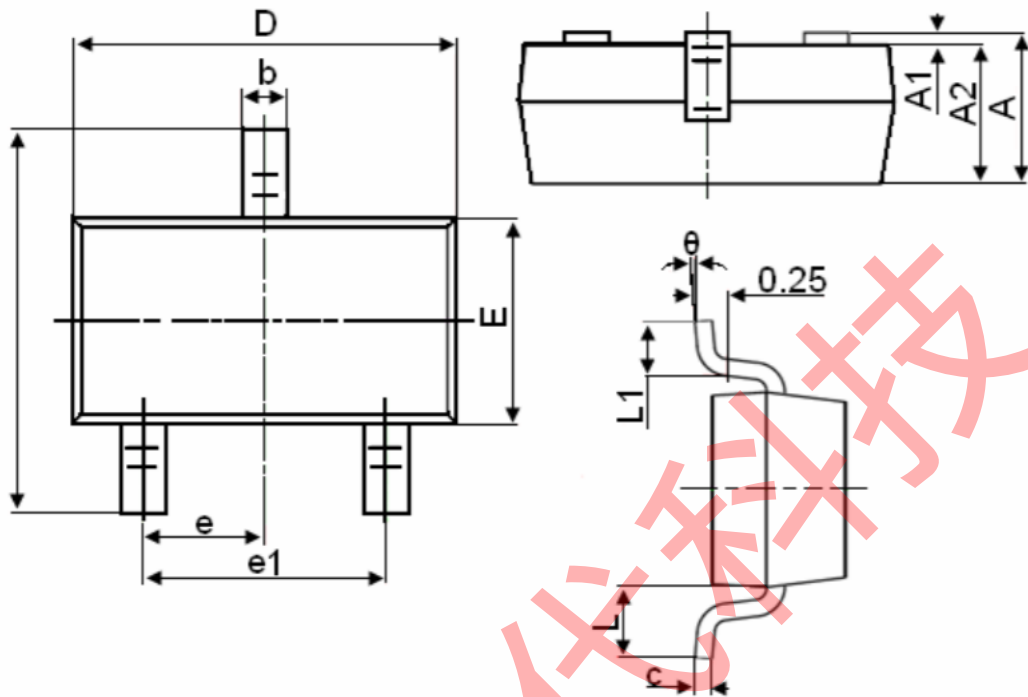


Figure 14 Normalized Maximum Transient Thermal Impedance

Package Information

- SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°