WT7131A
Synchronous Rectification Controller

Product Spec.

Rev. 0.1

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1. General Description

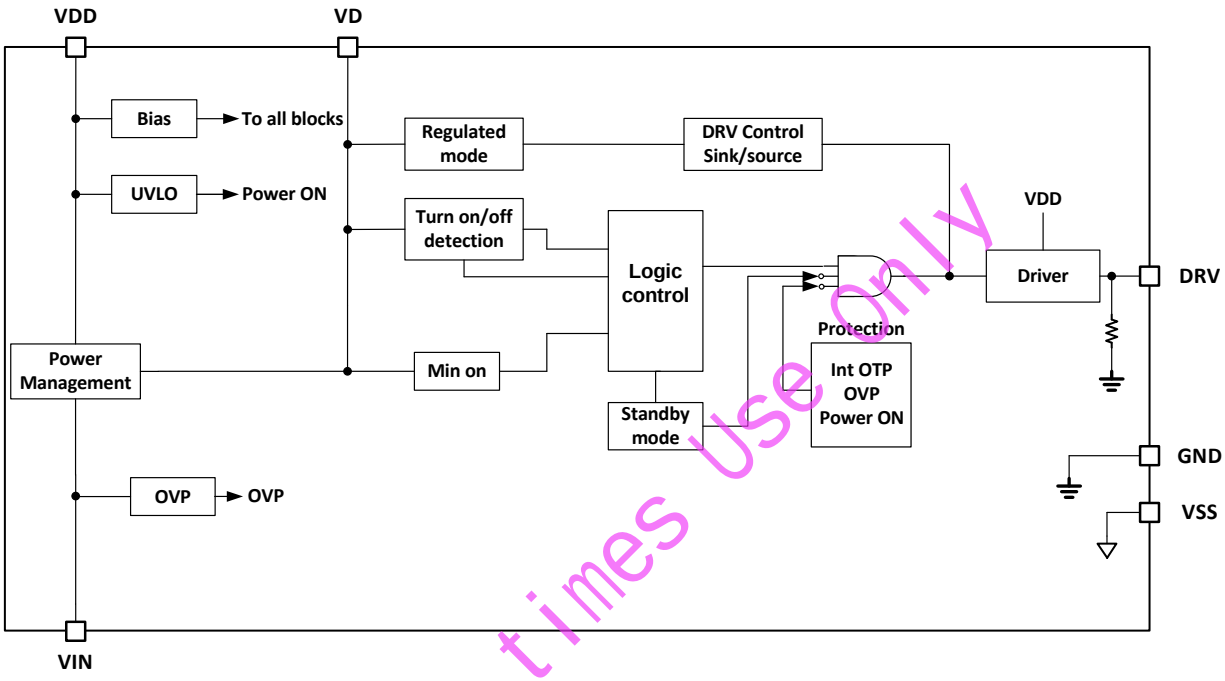
The WT7131A is a high-performance synchronous rectification controller. It is used to control a secondary-side synchronous rectification MOSFET in a flyback switch mode power supply. Without external auxiliary winding supplies, the WT7131A can easily provide power to the VDD. It can be powered by either the VIN or VD pin. The WT7131A built-in several circuits to minimize external part counts and overall total system cost.

By sensing the voltage across the conduction resistance of MOSFET, the controller can determine the turn-on/turn-off timing of the internal driver to achieve the lowest loss and high speed sensing. Due to the 200V voltage rating of VD pin, the controller is suitable for high output current and wide output voltage range application (e.g., PD3.0 and PPS, from 3.3V to 21V).

2. Features

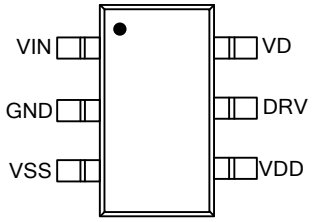
- Secondary side controller optimized for USB PD
- V_{DS} MOSFET direct-sensing (200V)
- Suspending for light load operating
- Low startup current
- Low operation current at standby mode
- Suitable for flyback CCM/DCM/QR/Valley switching operation
- No need the auxiliary winding
- Unique dynamic DRV control technology for fast turn off
- Outline package: SOT-26

3. Block Diagram



4. Pin Configuration

SOT-26



4.1 Pin Description

Pin No. SOT-26	Pin Name	Description
1	VIN	Input Voltage
2	GND	Ground connection. The PCB layout of the GND pin should as close as possible to the SOURCE terminal of external NMOSFET.
3	VSS	Connect to source of SR MOS.
4	VDD	Voltage source for internal control circuitry and SR gate driver
5	DRV	Gate drive for the external MOSFET
6	VD	MOSFET drain sensing. Series a resistor from DRAIN of MOSFET to VD pin is recommended to protect the controller prevent the controller from been damaged by the negative voltage of VD pin.

5. Functional Description

5.1 VDD Turn-on/off Section

When the VDD is below the VDD_OFF threshold, the controller is disabled and the SR-MOSFET will not turn on. It can serve as under voltage lock-out (UVLO) protection for the controller. When the VDD of WT7131A exceeds the VDD_ON level, the DRV will output the drive signal. Furthermore, when VDD pin voltage level exceeds the over voltage threshold, the controller will disable the DRV signal to protect the controller and MOSFET.

5.2 MOSFET On-off Control Logic

The VD and VSS are differential inputs used to sense the voltage across the drain-to-source voltage of SR-MOSFET. The control circuit of this controller determines the conduction time of external MOSFET by comparing the MOSFET's VDS voltage against the internal on/off threshold.

When the primary switch of a flyback converter turned off, the energy that stored in secondary winding starts to deliver the energy to the output capacitor and the output load. At this moment, the secondary body diode of SR MOSFET turned on and the inductor current flow through the body diode of MOSFET. This situation will let the VD pin voltage below the internal turn on threshold VTH_ON (-80mV Typ.). The controller starts to drive the MOSFET on with a minimum delay. The DRV output has a minimum on time to avoid the noise from turning off the driver. The secondary winding continuously to discharge the energy that stored in the winding. The discharge current gradually reduced and the VDS voltage drop also gradually reduced. Once the VD pin voltage reaches the dynamic gate control threshold (-30mV Typ.), the DRV pin of the WT7131A will be pulled low and the voltage drop VDS of SR MOSFET will be kept at the gate control level until the VDS of SR MOSFET is higher than VTH_OFF (-5mV Typ.). The controller turns off the MOSFET immediately. A turn-off blanking is applied when the DRV signal is pulled low. The turn-off blanking is removed when VDS rises above VRD_TH (3V).

5.3 Gate Drive

A gate driver has the capability to keep SR MOSFET turned-off even when there is no supply or low supply voltage for the SR controller. During the flyback topology switch mode power supply operation, SR MOSFET's drain voltage will goes up and down, and this may turn on SR MOSFET because the drain-to-gate voltage is built through the drain to gate capacitance, C_{DG}. The WT7131A provides enough energy to make the internal driver's sink transistor activated to close SR MOSFET.

5.4 Standby Mode

The criteria for operating in standby mode or normal operation are determined by the cumulative rectifier conduction time (Tdis_tot). If Tdis_tot is less than Tds1 (225μs) at Tnor (12ms), the SR controller will enter into the standby mode and the DRV output will be disabled. In standby mode, if Tdis_tot is greater than Tdis2 (90μs) which occurs within T_{STB} (3ms), the device will exit from the standby mode.

5.5 VDD POWER

The VDD is powered by either the VIN or VD pin. The VIN by way of power management regulates the VDD voltage at 5.15V. When the VIN cannot maintain VDD regulation, the VDD will drop down. Meanwhile, the VD by way of power management keeps the VDD voltage to 5.15V.

5.6 Layout Guideline

When the primary switch is turned off in a flyback converter, the secondary inductor discharges the energy that stored in secondary winding. The discharge current flowed through the SR MOSFET. The WT7131A internal control circuit senses the voltage drop condition of SR MOSFET through the VSS and VD pin to turn on and turn off the SR MOSFET. For proper drive the SR MOSFET, the PCB layout should be concerned. Refer to Figure 1. Following is the layout guide for WT7131A.

1. The VD pin should close and connect directly to the drain of SR MOSFET.
2. The VSS pin should close and connect directly to the source of SR MOSFET.
3. Keep the VD and VSS pin loop area as small as possible.
4. Add a low ESR ceramic capacitor as close to the VDD pin as possible.
5. In addition, minimized the high current loop area for better EMI.

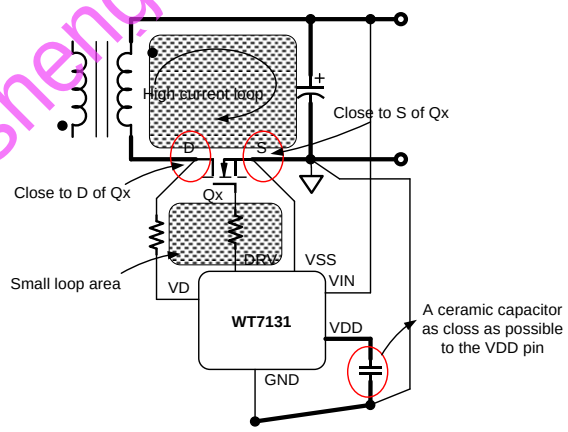


Figure 1

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DRV to GND	-0.3	Internal clamp	V
VDD to GND	-0.3	6	V
VD to GND	-1	200	V
VIN to GND	-0.3	30	V
Junction Temperature		150	℃
Operating Temperature	-40	125	℃
Storage Temperature Range	-55	150	℃
Lead Temperature (Soldering, 10 sec.)		260	℃
ESD Voltage Protection (Human Body Model), except VD pin	2.5		kV
ESD Voltage Protection (Human Body Model), VD pin	1		kV

NOTE: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected.

6.2 Recommended Operating Parameters

Parameter	Min.	Max.	Units
VIN		25	V
Maximum Junction Temperature		125	℃
VDD Capacitor	1	4.7	μF
The Resistor form the VD pin to the drain of SR MOSFET	22	470	Ω

Notes:

1. Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
2. The small signal components should be placed to IC pin as possible.
3. It's essential to connect VDD pin with a SMD ceramic capacitor to filter out the undesired switching noise for stable operation.

6.3 Thermal Characteristic

Package	Parameter		Min.	Typ.	Max.	Units
SOT-26	θ_{JA}	Thermal Resistance (Junction to Air)		175		°C/W
	T_{JMAX}	Maximum Junction Temperature		150		°C

6.4 Electrical Characteristic

(VDD=5V, T_A=25°C, unless otherwise specified)

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Voltage (VDD PIN)						
VDD_ON	VDD Turn-on Threshold		3.7	3.9	4.1	V
VDD_OFF	VDD Turn-off Threshold			3.5		V
IDD_ST	Startup Current			70		μA
IDD_STB	Operating Current in Standby Mode			200		μA
IVDD_OPE	Operating Current,	DRV=2.2nF, Fs=100kHz		2		mA
VDD_LDO	VIN LDO Output Voltage	VIN=6V		5.15		V
VDD_PLDO	VD LDO Output Voltage	VD=13V, VIN=0V		5.15		V
VIN_OVP	VIN OVP			28		V
	VDD OVP De_bounce Time.	(Note1)		120		μs
	OVP Hys.			3		V

Parameter		Test Condition	Min.	Typ.	Max.	Units
VDS Sensing (VD PIN)						
VD_ON	Turn ON Threshold			-80		mV
T_MIN_ON	Min. ON Time			0.5	0.59	μs
VDGC	Gate control threshold			-30		mV
VD_OFF	Turn OFF Threshold			-5		mV
VRD_TH	DRV ready threshold			3		V
TD_ON	Total Turn ON Delay	DRV=2.2nF		35		ns
TD_OFF	Total Turn OFF Delay	DRV=2.2nF		25		ns

Parameter		Test Condition	Min.	Typ.	Max.	Units
MOSFET Driver (DRV PIN)						
DRV_H	DRV High Level	VIN=6V,I=20mA	4.5		5.5	V
DRV_L	DRV Low Level	VIN=6V, I=100mA	0		0.3	V
T_{RISING}	Rising Time	DRV=2.2nF, DRV 1V→4V (Note1)		20		ns
$T_{FALLING}$	Falling Time	DRV=2.2nF, DRV 4V→1V (Note1)		8		ns

Parameter		Test Condition	Min.	Typ.	Max.	Units
Thermal Shutdown						
TSD	Thermal shutdown	Auto recovery mode, Note 1		150		℃
	Thermal shutdown Hys.	Note 1		25		℃

Note 1. Guaranteed by design.

7. Application Circuit

7.1 Type 1 Low side drive

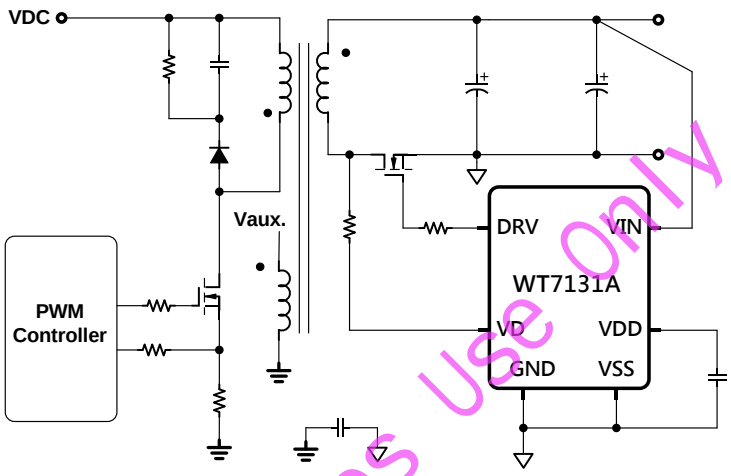


Figure 2

7.2 Type 2 High side drive

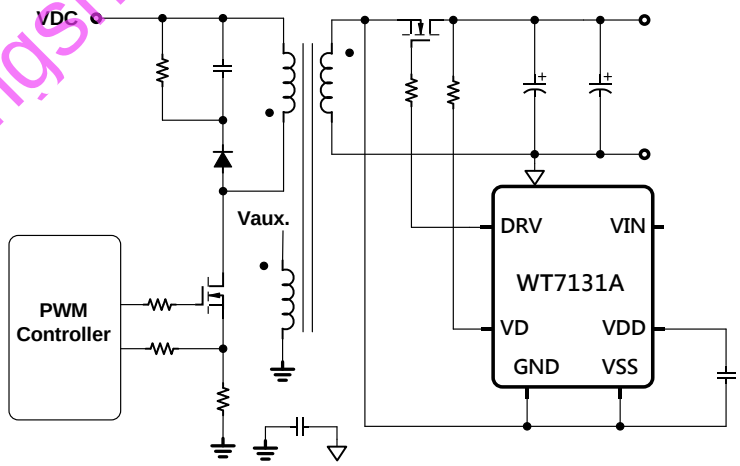


Figure 3

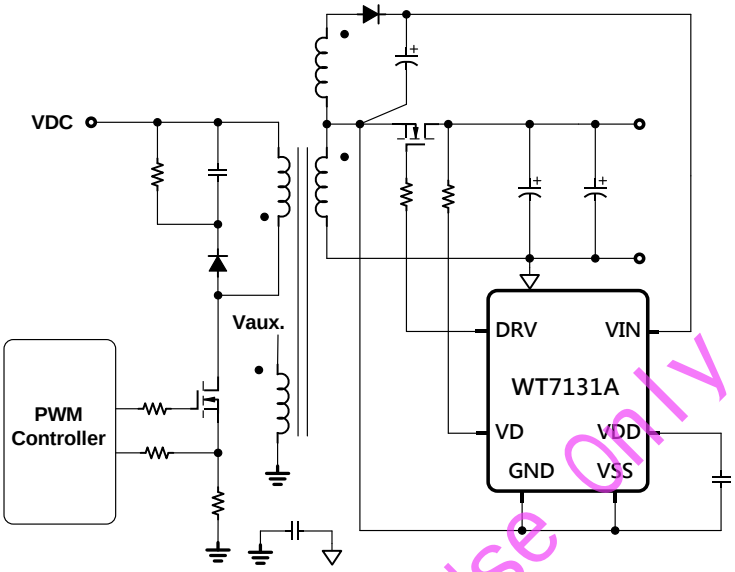
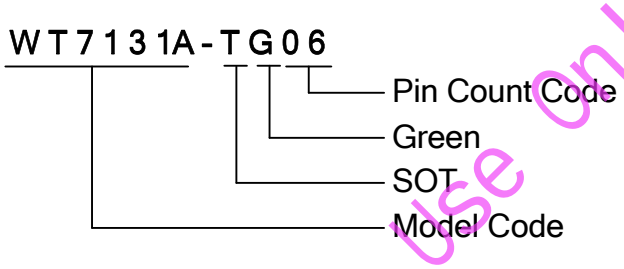
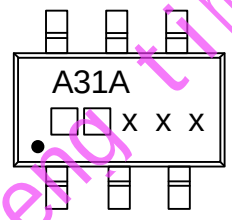


Figure 4

8. Ordering Information

Package Type	Part Number	Ordering Number	Top Mark	Tapping (EA/Reel)
SOT-26	WT7131A	WT7131A-TG06	A31A	3000





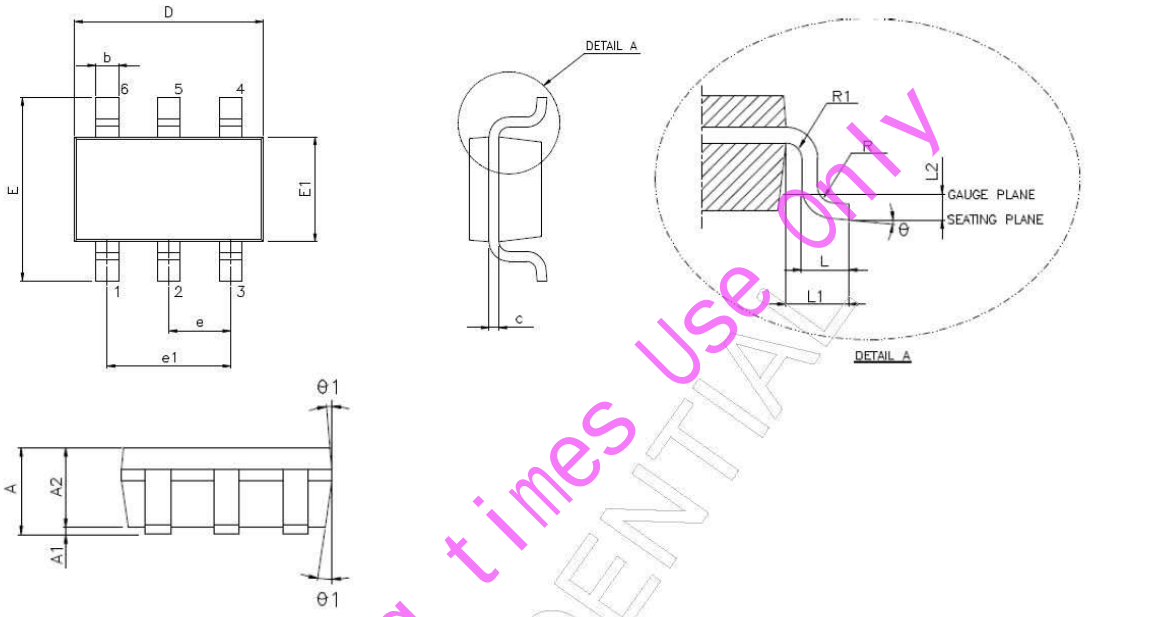
□□ : Date Code

x x x: Production Tracking Code

9. Package Information

9.1 Package Dimensions

Small Outline Transistor **SOT-26**



SYMBOLS	MIN	NOR	MAX
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
c	0.08	-	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ°	0	4	8
θ1°	5	10	15

UNIT: mm

NOTES:
1. JEDEC outline : MO-178 AB

PREPARE	Cynthia	DATE: 2012/7/25
CHECK	Lawrence	DATE: 2012/7/25
APPROVE	Eric	DATE: 2012/7/25

10. Revision History

Version	History	Date
0.1	Initial issue	September 2020