WT7162RH
Multi-Mode Flyback PWM Controller

Product Spec.

Rev. 0.4

August 2022

Weltrend Confidential for 通盛 Only

Copyright Notice

This data sheet is copyrighted by Weltrend Semiconductor, Inc. Do not reproduce, transform to any other format, or send/transmit any part of this documentation without the express written permission of Weltrend Semiconductor, Inc.

Disclaimers

Right to make change –
This document provides technical information for user. Weltrend Semiconductor, Inc. reserves the right to make change without further notice to any products herein.

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

Table of Contents

Weltrend Confidential for 建榮 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

1. General Description

The WT7162RH is a high frequency multi-mode (QR/Valley Switching) Flyback PWM controller. It is specifically designed to work with USB PD controller to provide a total solution for USB PD or a programmable power adapter. The WT7162RH helps to improve the overall efficiency and optimize the product performance. It operates in quasi-resonant (QR) mode during heavy load and operates in discontinuous conduction mode with valley switching during light load.

The WT7162RH minimizes the components counts and is available in a SOP-10/SOP-08 package. It provides important protection features, such as Brown In/Out, VDD OVP, OLP, OCP and Output Short Circuit Protection. Without an external LDO circuit, the WT7162RH can easily provide 3.3V~21V (7x volts) wide-range output voltage application to effectively reduce total BOM cost.

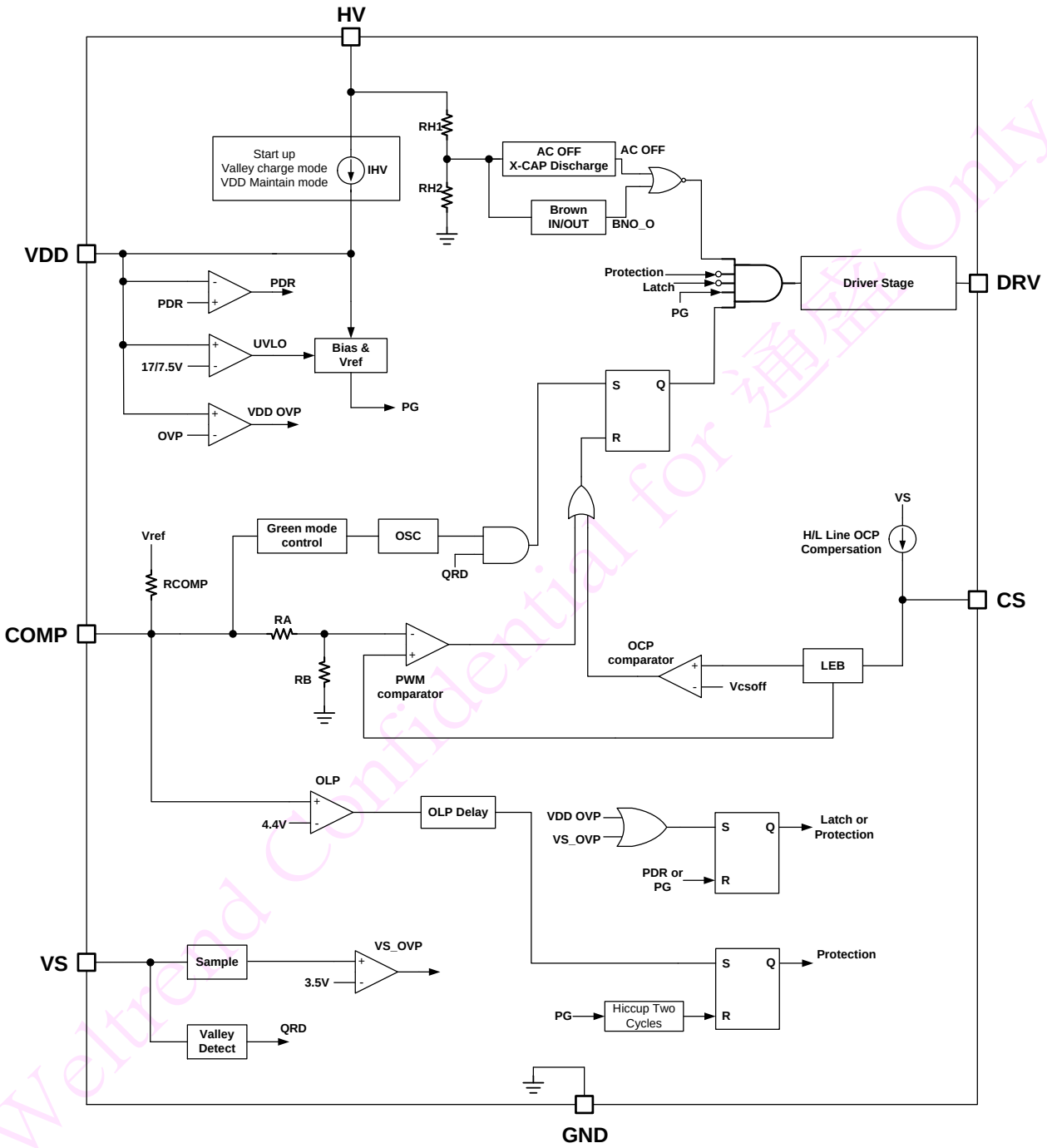
2. Features

- 180 kHz Max. Frequency Operation
- 700V Ultra HV Start-up Current
- Ultra HV Valley Charge Mode (VCM) for Wide Output Voltage Operation (USB PD 3.0 & PPS 3.3V~21V)
- Optimized for Wide Output Voltage
  - Adaptive OCP Compensation with Adjustable Line Compensation
  - Adaptive Green Mode Control
  - No External VDD Linear Regulator Circuit
  - Only One VDD Auxiliary Winding
- QR Mode/Valley-Switching Multi-Mode Operation
- Built-in X-Cap Discharge Function
- Internal Soft-Start Function
- Protection:
  - Brown In/Out Protection on HV Pin
  - Output Over Voltage Protection (VS_OVP)
  - VDD Over Voltage Protection (VDD_OVP)
  - Open Loop Protection (OLP) when Feedback Loop Open
  - Over Current Protection (OCP)
  - Internal Over Temperature Protection
  - CS Pin Open Protection
- Green Package: 10-pin/8-pin SOP

Weltrend Confidential for 通盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

3. Block Diagram

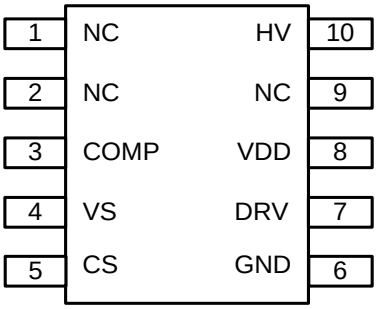


Weltrend Confidential for 通廠 Only

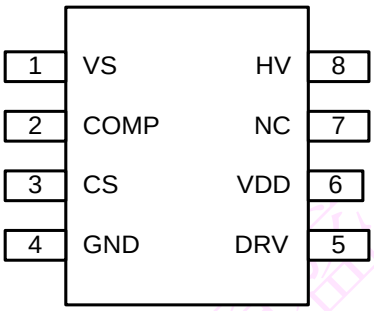
Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

4. Pin Configuration

10-pin SOP



8-pin SOP



4.1 Pin Description

Pin Number		Pin Name	Description
SOP10	SOP8		
1, 2, 9	7	NC	
3	2	COMP	This pin connects to a photo-coupler collector and adjusts the peak current set point. By a resistor between VDD and COMP pin, the brown in/out detect thresholds can be changed.
4	1	VS	This pin connects to a voltage divider between an auxiliary winding and detects the core demagnetization to have the controller operated at the valley switching for DCM. This pin provides the output over-voltage detection.
5	3	CS	The current sense pin monitors and control the primary peak current.
6	4	GND	Ground
7	5	DRV	This pin drives the gate of external MOSFET switch.
8	6	VDD	This pin is connected to an external auxiliary voltage and supplies the controller.
10	8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor and two diodes to provide the startup current for the controller. The HV pin also protects the converter when the input voltage lowers than the BNO level.

Weltrend Confidential for 通信 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

5. Function Description

The WT7162RH is a high frequency multi-mode (QR/Valley Switching) Flyback PWM controller. It is specifically designed to work with the USB PD controller or programmable power adapter controller, to provide a total solution. For the wide output voltage application, the WT7162RH features many new innovations, including UHV valley tracking charge mode, adaptive OCP compensation and adaptive green mode control. Its major features are described as below.

5.1 Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The WT7162RH is implemented with a high-voltage startup circuit for fast start-up functions and reduce power dissipations, as shown in Fig. 5.1. At startup, the high-voltage current source sinks current from AC Line and Neutral to provide startup current and charge the capacitor CVDD which connected to VDD. At the startup transient, the HV current will charge VDD capacitor until this VDD voltage reaches the UVLO (ON) threshold. As VDD trips UVLO (OFF), HV pin will recharge VDD capacitor till VDD voltage rises back to UVLO (ON) again. The resistor RHV connected in series with HV pin is recommended in the range between 100Ω and 510Ω. Besides, it is recommended that the VDD capacitor CVDD connected with VDD pin is in the range from 22μF to 47μF. It is important to note that it is not allowed to connect HV pin to any DC voltage. (e.g. directly to bulk capacitor)

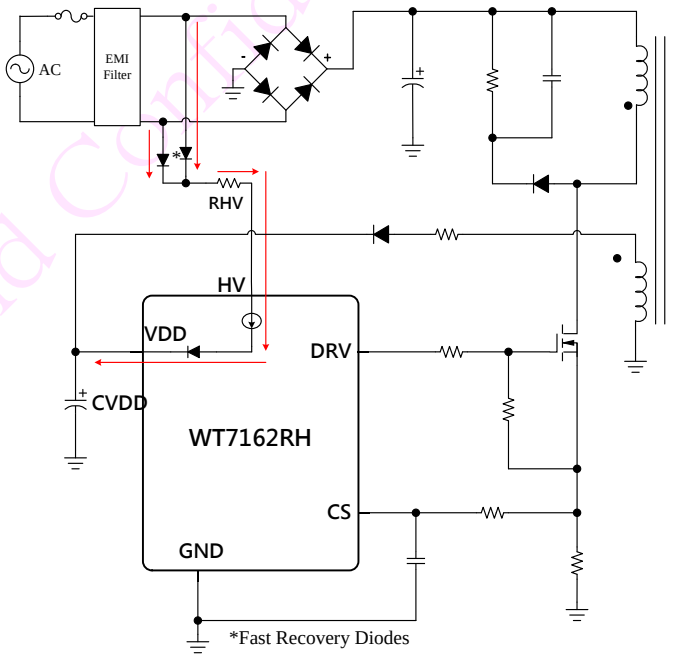


Fig. 5.1

Weltrend Confidential for 通盈 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

5.2 Brown In/Out Protection

The WT7162RH features brown in/out protection on HV pin. When HV pin voltage (VHV) goes above brown-in threshold (BNI) and VDD > VDD_BNO (13.5V), the controller can start immediately. Otherwise, the controller actually starts the next time VDD reaches UVLO (ON), as shown in Fig. 5.2. When VHV goes below brown out threshold (BNO) for more than a de-bounce time, the controller will stop switching.

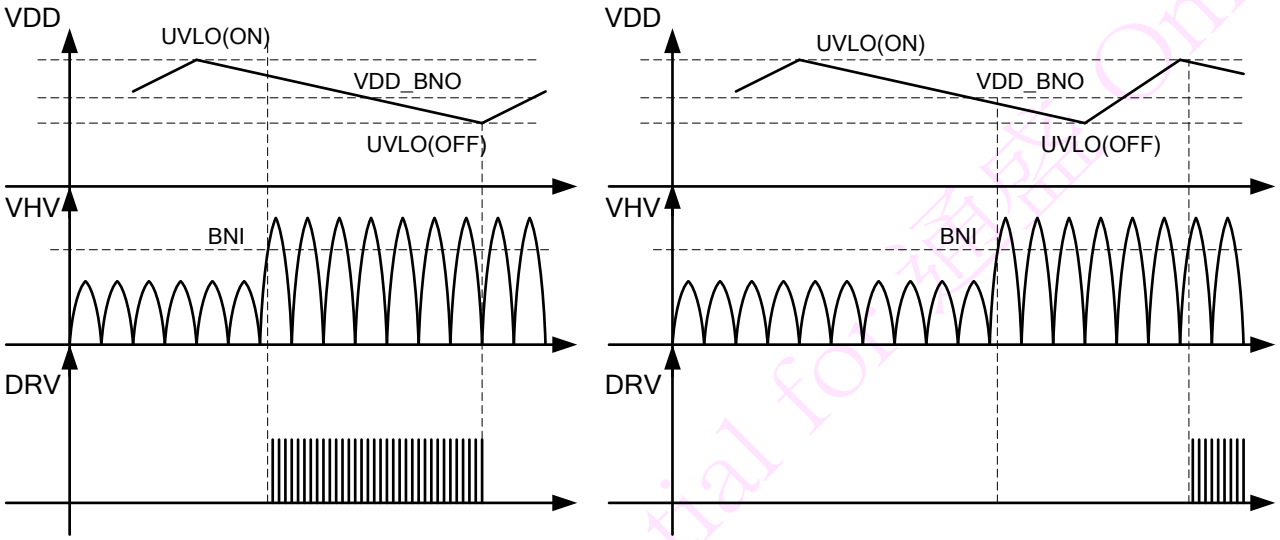


Fig. 5.2

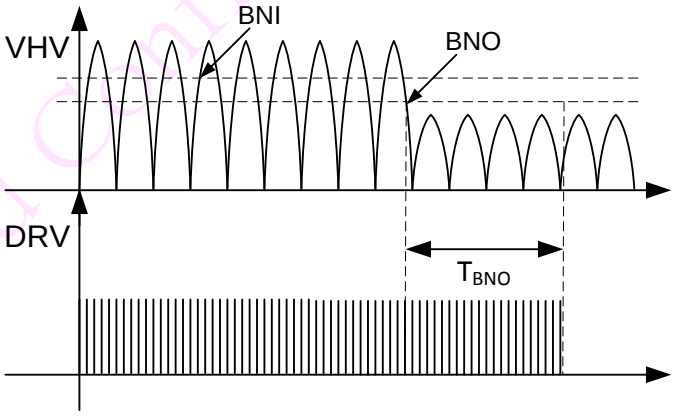


Fig. 5.3

Weltrend Confidential for 福昕 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

5.3 HV Valley Charge Mode & VDD Maintain Mode

For wide VOUT range application, the WT7162RH provides the HV pin valley charge mode (VCM). When VDD voltage is below the VDD_VCM (OFF) and HV voltage is below ON threshold (near the valley region), HV valley charge mode will be enabled. The HV VCM will supply current to keep the VDD voltage, as shown in Fig. 5.4. Therefore, the WT7162RH can reduce additional VDD LDO regulator circuits to have a better total BOM cost.

The VDD maintain mode can also turn on and turn off the HV current to maintain the VDD voltage no matter how high the HV voltage is. However, the HV current will be limited to 4mA (Typical) to protect the HV device.

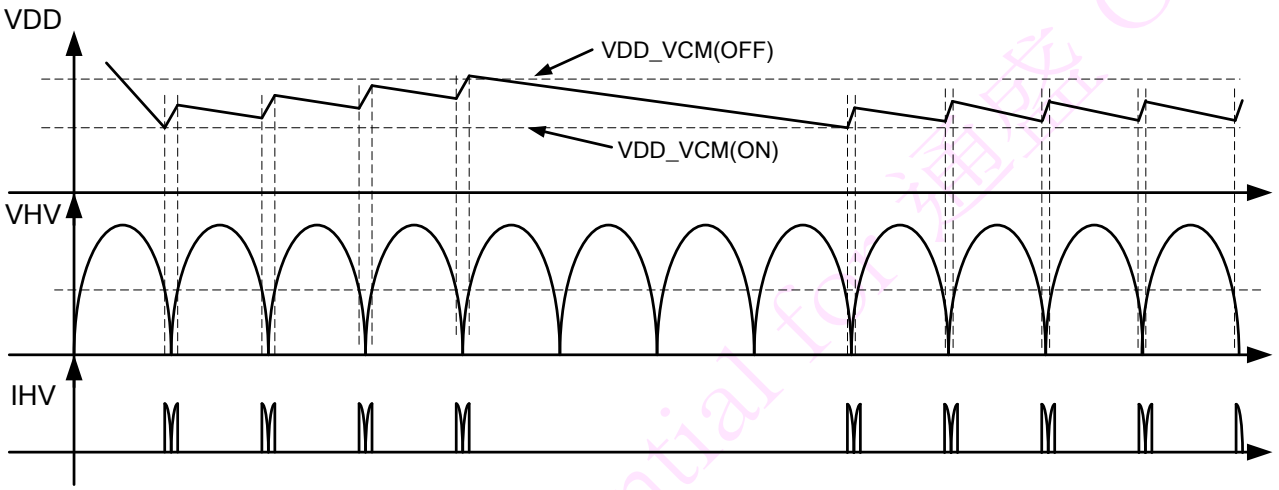


Fig. 5.4

5.4 HV X-Cap Discharge Function

In general, a discharging resistor is placed across X-capacitor to meet safety requirement. This component requires to be discharged in less than 1 second after AC line is disconnected. To eliminate the significant power loss from this discharging resistor, the IC applies the patent technology to discharge X-Cap's energy through HV current source when AC line is disconnected. By applying this technology, the system can easily pass the safety test without discharging resistor. When the X-Cap discharge function is enabled, the DRV will be off to stop the switching of power circuit. The IC will restart after the four VDD hiccup cycles.

5.5 Multi-Mode Operation for High Efficiency

The WT7162RH is a high performance multi-mode (QR/Valley Switching) Flyback PWM controller. The controller could operate in QR mode and DCM with valley switching. As the load decreases, the controller enters green mode with valley switching. At zero load or very light load conditions (V_{COMP} < Burst mode voltage), the DRV pin of the WT7162RH will be disabled immediately under such condition, enhancing power saving. The WT7162RH helps to improve the overall efficiency and optimize the product performance.

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

Weltrend Confidential for 潤峰 Only

5.6 Open Loop Protection (OLP)

The WT7162RH has an open loop protection function. An internal circuit detects the V_{COMP} level, when the V_{COMP} is larger than an OLP threshold level and continues over OLP delay time, the protection will be activated and then turn off the DRV output to stop the switching of power circuit. The IC will restart after two VDD hiccup cycles.

5.7 Gate Clamp

Driver output is clamped by an internal clamping circuit to prevent from undesired over-voltage gate signals to reduce the current consumption of the controller.

5.8 Output OVP on VS Pin

The WT7162RH provides the OVP by using VS pin, as shown in Fig. 5.5. It samples the auxiliary winding voltage via the divided resistors after a blanking time when DRV off. The auxiliary winding voltage is reflected to secondary winding and therefore the voltage on the VS pin is proportional to the output voltage. The sampling voltage level, VS, is used for OVP. If VS exceeds the 3.5V, the VS OVP circuit switches the power MOSFET off. The equation of VS is shown as below:

$$VS = Vaux \times \frac{R2}{R1 + R2} = Vout \times \frac{Naux}{Ns} \times \frac{R2}{R1 + R2}$$

$$R2 = \frac{R1}{\frac{Vout\_OVP}{3.5} \times \frac{Naux}{Ns} - 1}$$

Where Naux is the turns of VDD winding, Ns is the turns of secondary winding.

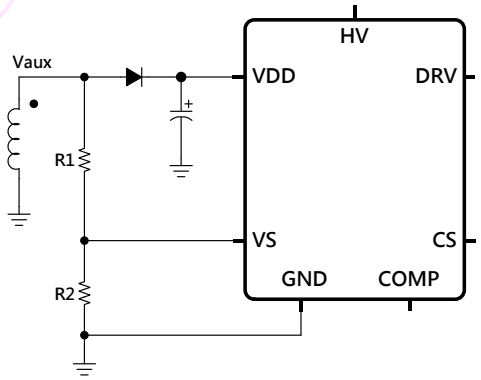


Fig. 5.5

Weltrend Confidential for 通盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

5.9 Adaptive Over Current Compensation

To compensate over current protection under different input voltage, an offset voltage is added to the CS signal by an internal current source, IOCP and an external resistor, Rcs, in series between the sense resistor, RS, and the CS pin, as shown in Fig. 5.6. Different values of resistors in series with the CS pin may adjust the amount of compensation. The value of IOCP depends on the clamping current, IVS, of VS pin when the MOSFET is turned on. The clamping current is proportional to the input voltage. The relationship between IOCP and IVS is shown as Fig. 5.7. The equation of IVS and R1 are decreased as:

$$IVS = \frac{Vaux}{R1} = \frac{Vin \times Naux / Np}{R1}$$

Where Np is the turns of primary winding.

The WT7162RH also could adjust down the current limit (VCS_OFF) if it detects a lower output voltage by detect the VS pin voltage. Therefore, the WT7162RH can help the system easily pass the LPS spec.

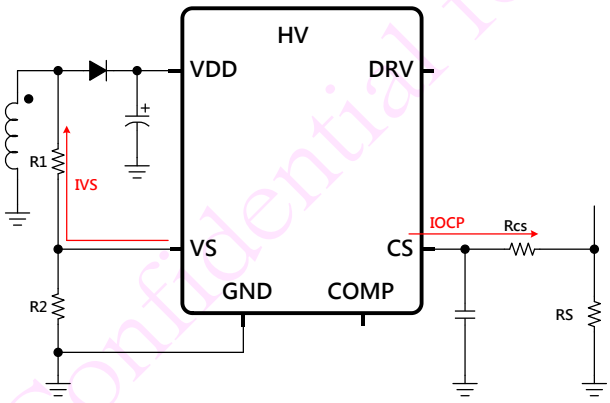


Fig. 5.6

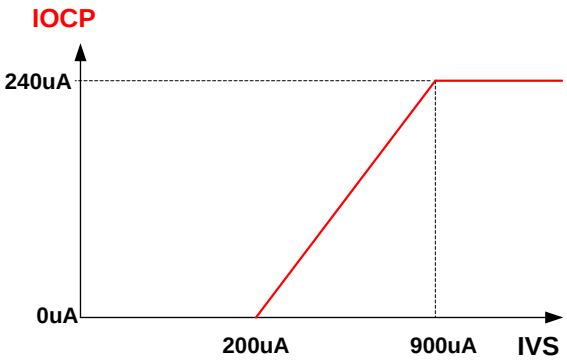


Fig. 5.7

Weltrend Confidential for 通盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

Table 5.1

VCS_OFF_1	9-20V OCP	VS>1.1V	0.66V
VCS_OFF_2	5V OCP	VS>0.7V	0.60V
VCS_OFF_3	3V OCP	VS<0.7V	0.56V

5.10 Adaptive Green Mode Control

By using the green-mode control, the maximum switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency at light load. The system stability is different for wide range VOUT range application. The WT7162RH would adjust green mode curve automatically to ensure the system stability for different VOUT operation. When VS pin voltage < 1.0V, the green mode curve period will be increased to improve system stability for lower output voltage, as shown in Fig. 5.8.

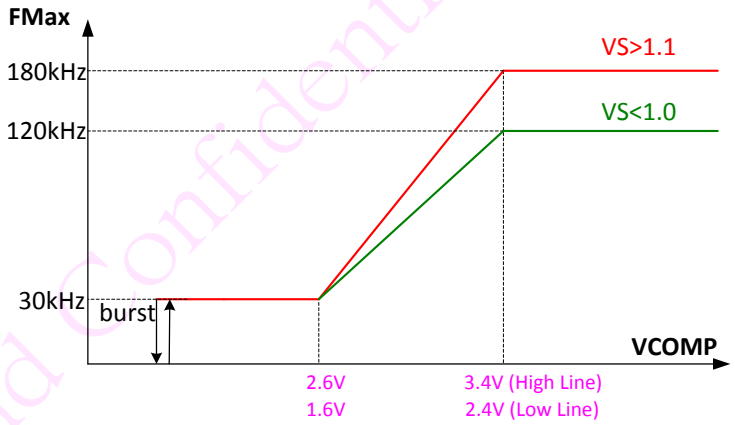


Fig. 5.8

Weltrend Confidential for 建盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
HV Pin	-0.3	700	V
VDD to GND	-0.3	41	V
DRV to GND	-0.3	Internal clamp	V
VS, COMP, CS,	-0.3	6.5	V
VS (Transient Time ≦1μs)	-1	6.5	V
Junction Temperature		150	℃
Lead Temperature (Soldering, 10 sec.)		260	℃
Storage Temperature Range	-65	150	℃
MM ESD (except HV Pin)	300		V
HBD ESD (except HV Pin)	3		kV
MM ESD (HV Pin)	300		V
HBD ESD (HV Pin)	1		kV

NOTE: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected.

6.2 Recommended Operating Parameters

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
AC Input Voltage Range	Vac		63		264	Vrms
V_{DD} Capacitor	CVDD		22		47	μF
HV Pin Resistor	RHV		100		510	Ω
COMP Pin Capacitor	C_{COMP}		0.1		4.7	nF
Operating Junction Temperature	T_J		-40		125	℃

Notes:

- Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
- The small signal components should be placed to IC pin as possible.
- It's essential to connect VDD pin with a SMD ceramic capacitor (0.1μF~1.0μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.

Weltrend Confidential for 建碁 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

6.3 Thermal Resistance

Package	Parameter		Min.	Typ.	Max.	Units
10-pin SOP	θ_{JA10}	Thermal Resistance (Junction to Air)		88		°C /W
	θ_{JC10}	Thermal Resistance (Junction to Case)		37		°C /W
8-pin SOP	θ_{JA08}	Thermal Resistance (Junction to Air)		150		°C /W
	θ_{JC08}	Thermal Resistance (Junction to Case)		39		°C /W

6.4 Version Table

Protection	WT7162RH
VDD OVP	Auto
VS OVP	Auto
OLP	Auto (Hiccup Two Cycles)

6.5 Electrical Characteristics

(VDD=15V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High Voltage Startup (HV PIN)						
HV Startup Current	IHV_ST_0	HV=100V, VDD=0V		1		mA
HV Startup Current	IHV_ST_1	HV=100V, VDD=15V		2.7		mA
HV Pin Leakage Current	IHV_LK_1	HV=500V, VDD_ON & HV Current OFF		32		μA
HV Pin Brown IN Threshold	VHV_BNI	VCC to COMP=NC	105	113	121	V_{DC}
HV Pin Brown OUT Threshold	VHV_BNO	VCC to COMP=NC	95	102	109	V_{DC}
Brown IN De-bounce Time	TBNO_IN	(Note1)		128		μs
Brown OUT De-bounce Time	TBNO_OUT	(Note1)		64		ms
X-Cap Discharge De-bounce Time	THV_DIS	(Note1)		64		ms

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage (VDD PIN)						
VDD Turn-on Threshold	VDD_ON		16	17	18	V
VDD Turn-off Threshold	VDD_OFF		7	7.5	8	V
Startup Current	IDD_ST	VDD=V_{DD_ON}-0.2V		80		μA

Weltrend Confidential for 瑞盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Current	IVDD_0	COMP=0V		500		μA
Operating Current	IVDD_3	DRV=1nF, COMP=3V, VS=2Vdc		1.9		mA
HV Valley Charge Mode ON	VDD_VCM_ON	(Note1)		12.5		V
HV Valley Charge Mode OFF	VDD_VCM_OFF	(Note1)		14.5		V
VDD Maintain Mode ON Level	VDD_Main	(Note1)		8.5		V
VDD Maintain Mode OFF Level	VDD_Main_OFF	(Note1)		11		V
VDD OVP	VDD_OVP		37.5	39	40.5	V
VDD OVP De_bounce Time				4		cycle
Protection Current_Auto	IPROT_A			320		μA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Loop Compensation (COMP PIN)						
COMP Open Level	VCOMP_OPEN		5	5.3	5.6	V
Open Loop Trip Threshold	VOLP		4.2	4.4	4.6	V
COMP Short Current	ICOMP_0V		170	200	230	μA
AV For CS/COMP		RA/RB, (Note1)		5.5		
Burst ON Threshold	Burst_ON1	VS<1.5V	0.7	0.8	0.9	V
Open Loop Delay Time	TOLP	after start-up	68	80	92	ms

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Internal Oscillator						
Max. Switching Frequency	FMax	V_{COMP}=3V, VS>1.1V	170	180	190	kHz
Green Mode Frequency	FGREEN			30		kHz
FMax Jitter Range	FJitter			-20		%
Maximum ON Time	TMAXON		12	13.5	15	μs
Time Out	TO2			20		μs

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Current Sense (CS PIN)						
CS OFF Threshold,	VCS_OFF1	VS>1.1V	0.64	0.66	0.68	V
Leading Edge Blanking	TLEB	For OCP (Note1) Included DRV Delay		250		ns
Soft Start	TSS1	(Note1)		5		ms

Weltrend Confidential for 偉詮 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
MOSFET Driver (DRV PIN)						
DRV High Level	VOH	RL=1kΩ	9.5		VDD	V
DRV Low Level	VOL	Io=40mA	0		1	V
DRV Clamp Level	VOC	RL=1nF//10 kΩ		12		V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Valley Switching (VS PIN)						
VS_OVP Threshold	VS_OVP		3.36	3.5	3.64	V

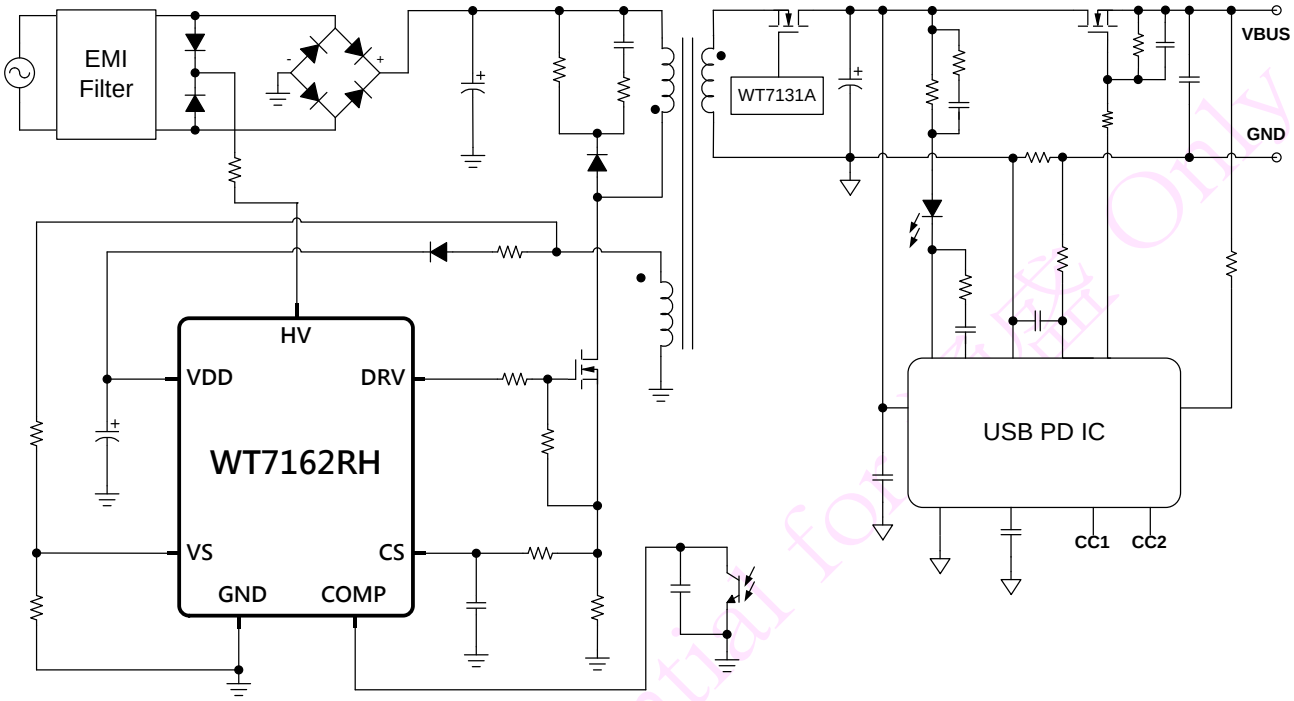
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Internal Thermal Shutdown						
Thermal shutdown temperature	T_{SD_L}	(Note1)		150		℃

Note 1. Guaranteed by design.

Weltrend Confidential for 通富 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

7. Simplified Application Circuit



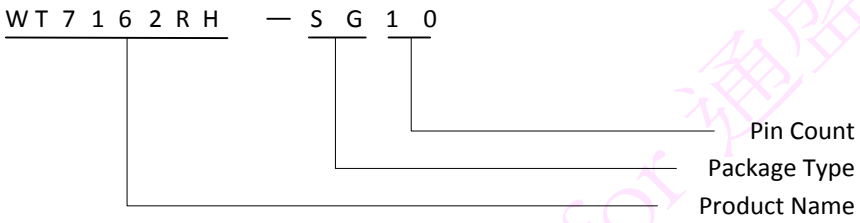
Weltrend Confidential for 客戶 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

8. Ordering Information

Part Number	Package Type	Ordering Number	Tapping (EA/Reel)
WT7162RH	SOP-10	WT7162RH-SG10	4000
WT7162RH	SOP-08	WT7162RH-SG08	4000

Example



Top Marking

10-pin/8-pin SOP Top Marking

□: Date Code

X: Production Tracking Code

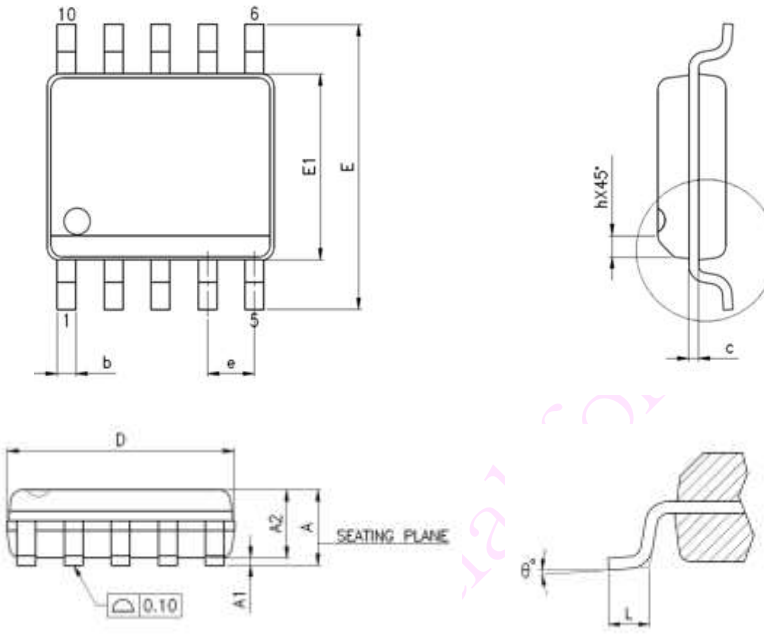
Weltrend Confidential for 通盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

9. Package Information

9.1 Package Dimensions

10-pin SOP



All dimensions shown in mm

SYMBOL	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.30	0.45
c	0.10	0.25
D	4.80	4.95
E	6.00 BSC	
E1	3.80	4.00
e	1.0 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

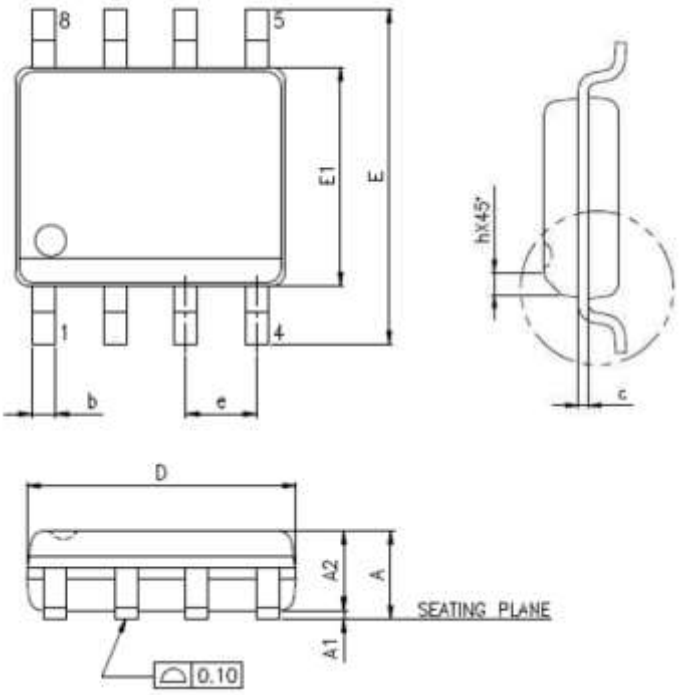
Notes:

1. JEDEC outline: MS-012 AA REV.F
2. Dimension “D” does not include mold flash, protrusions or gate burrs mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

Weltrend Confidential Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

8-pin SOP



All dimensions shown in mm

SYMBOL	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

Notes:

1. JEDEC outline: MS-012 AA REV.F
2. Dimension “D” does not include mold flash, protrusions or gate burrs mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

Weltrend Confidential 盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.

10. Revision History

Version	History	Date
0.1	Initial issue	April 2021
0.2	Update “Features”, CH5.9, CH5.10, and CH6.5	September 2021
0.3	Add SOP-08 package Update “Application Circuit”	November 2021
0.4	Update “Features”, CH5.2, CH6.1 and CH6.5	August 2022

Weltrend Confidential for 通盛 Only

Copyright© 2022 Weltrend Semiconductor, Inc. All Rights Reserved.
Weltrend reserves right to modify all information contained in this document without notice.