APM
A Power Microelectronics

AP150N20MP
200V N-Channel Enhancement Mode MOSFET

Description

The AP150N20MP uses advanced Trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 12V. This device is suitable for use as a Battery protection or in other Switching application.
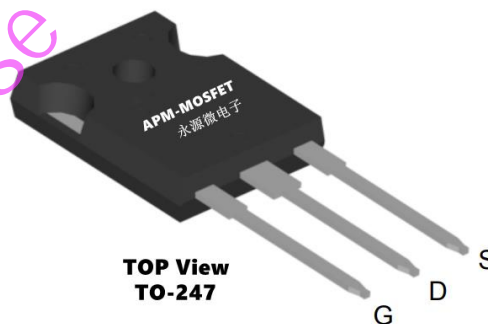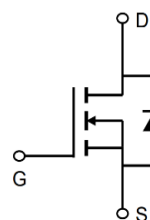
General Features

V_{DS} = 200V I_D =150A

$R_{DS(ON)}$ < 10mΩ @ V_{GS}=10V **(Type：8.5mΩ)**

Application

UPS

inverter

**TOP View
TO-247**

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP150N20MP	TO-247-3L	AP150N20MP XXX YYYY	300

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDSS	Drain-to-Source Voltage	200	V
ID@TA=25℃	Continuous Drain Current VGS @ 10V	150	A
ID@TA=70℃	Continuous Drain Current VGS @ 10V	102	A
IDM[a1]	Pulsed Drain Current (pulse width limited by T_{JM})	450	A
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy	1600	mJ
EAra1	Avalanche Energy, Repetitive	150	mJ
IAR a1	Avalanche Current	90	A
dv/dt[a2]	Peak Diode Recovery dv/dt	10.0	V/ns
PD	Power Dissipation	750	W
TJ，Tstg	Operating Junction and Storage Temperature Range	150，−55 to 150	℃
TL	Maximum Temperature for Soldering	300	℃
RθJC	Thermal Resistance, Junction-to-Case	0.45	℃/ W
RθJA	Thermal Resistance, Junction-to-Ambient	40	℃/ W

AP150N20MP RVE1.0

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Electrical Characteristics@T$_j$=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDSS	Drain to Source Breakdown Voltage	V$_{GS}$=0V, I$_D$=250µA	200	220	--	V
IDSS	Drain to Source Leakage Current	V$_{DS}$=200V, V$_{GS}$=0V,T$_a$=25°C	--	--	1.0	µA
		V$_{DS}$=200V, V$_{GS}$=0V,T$_a$=125°C	--	--	100	µA
IGSS(F)	Gate to Source Forward Leakage	V$_{GS}$=+20V	--	--	100	nA
IGSS(R)	Gate to Source Reverse Leakage	V$_{GS}$=-20V	--	--	-100	nA
RDS(ON)	Drain-to-Source On-Resistance	V$_{GS}$=10V, I$_D$=80A	--	8.5	10	mΩ
VGS(TH)	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$, I$_D$=250µA	3.6	4.3	5.0	V
gfs	Forward Trans conductance	V$_{DS}$=25V, I$_D$=80A	50	65	--	S
R$_g$	Gate Resistance	V$_{GS}$=0V V$_{DS}$ open f=1.0MHz		1.3		Ω
Ciss	Input Capacitance	V$_{GS}$=0V V$_{DS}$=25V f=1.0MHz	--	15000	--	pF
Coss	Output Capacitance		--	1000	--	pF
Crss	Reverse Transfer Capacitance		--	420	--	pF
td(ON)	Turn-on Delay Time	I$_D$=80A, V$_{DS}$=50V V$_{GS}$=10V, R$_g$=2.5Ω	--	90	--	ns
t$_r$	Rise Time		--	140	--	ns
td(OFF)	Turn-Off Delay Time		--	220	--	ns
tf	Fall Time		--	180	--	ns
Q$_g$	Total Gate Charge	I$_D$=80A, V$_{DD}$=100V V$_{GS}$=10V	--	170	--	nC
Qgs	Gate to Source Charge		--	30	--	nC
Qgd	Gate to Drain ("Miller") Charge		--	50	--	nC
ISD	Continuous Source Current (Body Diode)		--	--	150	A
ISM	Maximum Pulsed Current (Body Diode)		--	--	500	A
VSD	Diode Forward Voltage	I$_S$=80A, V$_{GS}$=0V	--	--	1.2	V
trr	Reverse Recovery Time	I$_S$=60A,T$_j$=25°C, V$_{DD}$=50V dI$_F$/dt=100A/µs, V$_{GS}$=0V	--	220	--	ns
Q$_{rr}$	Reverse Recovery Charge		--	1.1	--	uC

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is TJ = 25°C, L = 0.3mH, R$_G$ = 25Ω, V$_{DD}$=50V, V$_{GS}$=10V a2

4、The I$_{SD}$=80A,di/dt≤100A/us, V$_{DD}$≤BV$_{DS}$, Start T$_J$=25°C

5、The data is theoretically the same as I$_D$ and I$_{DM}$, in real applications , should be limited by total power dissipation.

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Package Mechanical Data-TO-247-3L
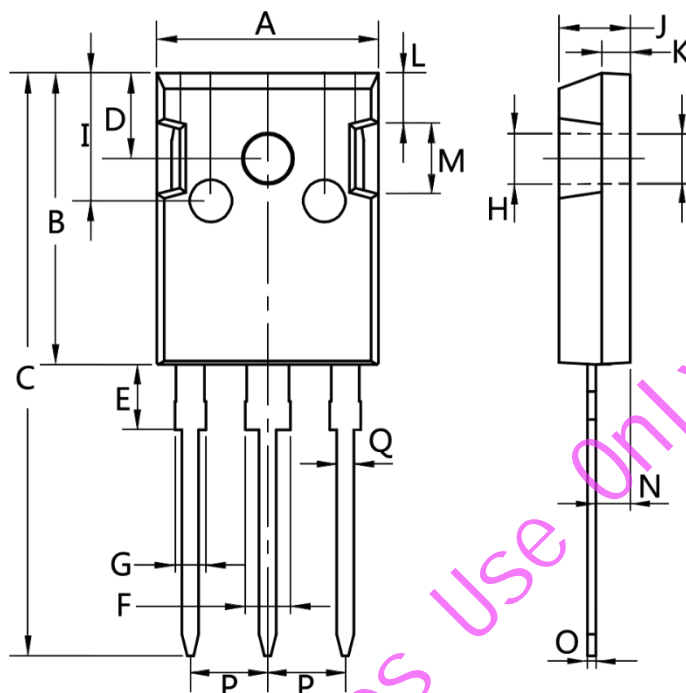
Dim.	Min.	Max.
A	15.0	16. 0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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AP75N20P/T

200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/10/31	Initial release

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