JW1515HA

Offline QR GaN Flyback Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW1515HA is a controller for offline flyback with GaN, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation. An internal frequency limitation is utilized to overcome the inherent disadvantages of QR flyback.

The JW1515HA combines PWM and PFM control at different input and load condition for highest average efficiency.

The JW1515HA comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption. It can comply with the most stringent efficiency regulations. Also, the HV pin is used for X-cap discharge when AC input is removed, which helps to reduce X-cap discharge loss and achieve extremely low standby power loss.

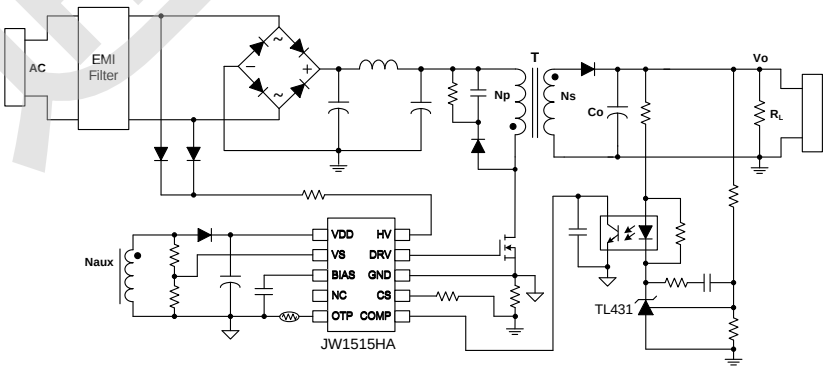
FEATURES

- Built-in High-Voltage Startup
- 6V Drive Voltage for GaN
- X-Capacitor Discharge Function
- Wider VDD Operation Range
- QR Operation for High Efficiency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP, Brown-In and Brown-Out, CS Open Protection, OCP, OPP, OLP, Internal OTP, External OTP
- Frequency Jitter to Ease EMI Compliance
- Available in SSOP-10 Package

APPLICATIONS

- PD and Quick-Charging Chargers
- AC/DC Adapters with Wide Output Range Chargers

TYPICAL APPLICATION



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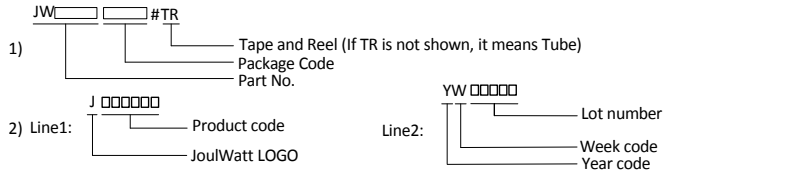
ORDER INFORMATION

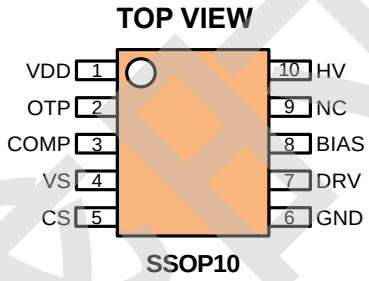
DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1515HASSOP#TR	SSOP10	J1515HA YW□□□□□	Green

Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

HV Voltage 700V
VDD Voltage 95V
OTP, COMP, CS Voltage Range ..... -0.3V to 5V (5V to 5.5V<10us)
DRV, BIAS Voltage Range ..... -0.3V to 6.3V (6.3V to 7V<10us)
VS Voltage Range ..... -0.3V to 5V (-0.7V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2)] 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC
Continuous Power Dissipation (T_A = 25 ºC)[3)] SSOP10 ..... 960mW

RECOMMENDED OPERATING CONDITIONS[4)]

VDD Voltage ..... 8 to 83V
Operating Junction Temperature (T_J) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{JC}
SSOP10	130	80°C/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1515HA includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

T_A = 25ºC, unless otherwise stated.

Advance Information, not production data, subject to change without notice.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
High Voltage Section (HV Pin)						
Supply Current from HV Pin	I_{HV}	V_{HV}=120V, V_{VDD}=0V	2.5	3	3.5	mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=500V, V_{VDD}=20V		20	30	uA
Brown-In Threshold	V_{BR_IN}	V_{HV} increasing	106	112	118	V
Brown-Out Threshold	V_{BR_OUT}	V_{HV} decreasing	91	97	103	V
Brown-Out Blanking Time[6]	t_{BR_OUT}			70		ms
Supply Voltage Section (VDD Pin)						
Turn-On Threshold Voltage	V_{DD_ON}	V_{VDD} increasing	15.5	16.5	17.5	V
Turn-Off Threshold Voltage	V_{DD_OFF}	V_{VDD} decreasing	7	7.8	8.5	V
Reset Threshold Voltage	V_{DD_RST}	Fault State	4	4.75	5.5	V
Startup Current	I_{DD_ST}	V_{VDD}=V_{DD_ON}-0.5 V		300	350	uA
Operating Supply Current	I_{DD_OP}	V_{VDD}=20V, f_S=f_{max}	0.7	0.75	0.8	mA
VDD OVP Voltage	V_{DD_OVP}	V_{VDD} increasing	85	90	94.5	V
Voltage Sense Section (VS Pin)						
Maximum VS Source Current Capability	I_{VS_MAX}	V_{VS}=-0.4V	2.7	2.9	3.1	mA
Adaptive Blanking time for VS Sampling[6]	t_{VS_BLK}	V_{COMP}=0.55V		0.6		us
		V_{COMP}=4V		1.2		us
Output OVP threshold	V_{VS_OVP}	V_{VS} increasing	2.8	3	3.2	V
Output OVP Debounce Cycle Counts[6]	N_{VS_OVP}	Fault State		3		Cycle
Current Sense Section (CS Pin)						
Max CS Offset Current	I_{CS_MAX}	V_{COMP}=4V	96	100	104	uA
Min CS Offset Current	I_{CS_MIN}	V_{COMP}=0V at Burst Mode	23	28	33	uA
CS Off Threshold	V_{CS_TH}	V_{CS} decreasing	0	30	60	mV
Leading-Edge Blanking Time[6]	t_{LEB}	V_{CS}=0		220		ns
OCP Enable Threshold[6]	V_{OCP_EN}			0.65		V
OCP Internal Threshold[6]	V_{OCP}			0.2		V
OCP Blanking Time[6]	t_{OCP_BLK}	Fault State		120		ms
Auto-Restart Cycles for OCP[6]	N_{OCP_HIC}	Fault State		4		Cycle
Frequency Jittering Section						
Frequency Jittering Amplitude to COMP[6]	ΔF_{JIT}			±7%		
Counting Cycles for Jittering[6]	N_{JIT_CYC}			32		Cycle
Drive Section (DRV Pin)						

Gate Output Voltage Low	V_{DRV_L}	Gate Off			0.5	V
Gate Output Clamping Voltage	V_{DRV_CLAMP}	Gate On	5.8	6	6.1	V
Maximum Source Current[6)]	I_{SRC}			100		mA
Maximum Sink Current[6)]	I_{SINK}			800		mA
Maximum ON Time	T_{ON_MAX}		15	17.5	20	us
Minimum ON Time	T_{ON_MIN}		245	280	315	ns
Maximum Switching Cycle	T_{S_MAX}		50	60	70	us
Maximum Switching Frequency	f_{max}	V_{COMP}=3.5V	178	190	202	kHz
Minimum Switching Frequency	f_{min}	V_{COMP}=0.8V	23	25	28.5	kHz
Feedback Section (COMP Pin)						
Open Pin Voltage[6)]	V_{COMP_MAX}	Open Loop		4		V
Internal Pull-Up Resistor[6)]	R_{COMP_UP}			20		kΩ
COMP to CS offset current Gain[6)]	G_{COMP_CS}	V_{COMP}>2.8V		20		V/mA
		V_{COMP}<1.0V		16		V/mA
The Threshold Enter PFM Mode	V_{COMP_PFM}	V_{COMP} decreasing		2.8		V
The Threshold Enter Burst Mode	V_{BUR_L}	V_{COMP} increasing	0.45	0.5	0.55	V
The Threshold Exit Burst Mode	V_{BUR_H}	V_{COMP} increasing	0.56	0.6	0.64	V
OPP Internal Threshold[6)]	V_{OPP}			0.8		V
OPP Blanking Time[6)]	t_{OPP_BLK}	Fault State		120		ms
Auto-Restart Cycles for OPP[6)]	N_{OPP_HIC}	Fault State		4		Cycle
Over Load Protection Threshold[6)]	V_{OLP}	V_{COMP} increasing		3.7		V
OLP Blanking Time[6)]	t_{OLP_BLK}	Fault State		120		ms
Auto-Restart Cycles for OLP[6)]	N_{OLP_HIC}	Fault State		4		Cycle
External Over Temperature Protection (OTP Pin)						
Over Temperature Protection (OTP) Enter Threshold	V_{OTP_IN}	V_{OTP} decreasing	235	250	270	mV
Over Temperature Protection (OTP) Exiting Threshold	V_{OTP_OUT}	V_{OTP} increasing	470	500	520	mV
OTP Pull-Up Current Source	I_{OTP}		22	27	32	uA
Internal Over Temperature Protection						
Thermal Shutdown Threshold[6)]	T_{OTP}	Internal junction temperature		140		°C
OTP Hysteresis[6)]	T_{HYS}	Internal junction temperature		30		ºC

Notes:

6) Guaranteed by design.

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PIN DESCRIPTION

PIN SSOP10	NAME	DESCRIPTION
1	VDD	Bias power input to the controller. A hold-up capacitor to GND is required.
2	OTP	External temperature sensing pin. An external NTC (negative temperature coefficient) thermistor to GND is required.
3	COMP	Feedback input pin for flyback QR controller. Connect to an opto-coupler.
4	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP. This pin also detects the resonant valley for QR operation.
5	CS	Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP function at the initial start.
6	GND	The ground of the IC.
7	DRV	Gate output pin.
8	BIAS	Bias power of the driver, an external hold-up capacitor to GND is required
9	NC	
10	HV	High voltage input pin. This pin provides source current to charge VDD. This pin is used for X-cap discharge when AC input is removed. Besides, this pin also senses input voltage for brown-in and brown-out protection.

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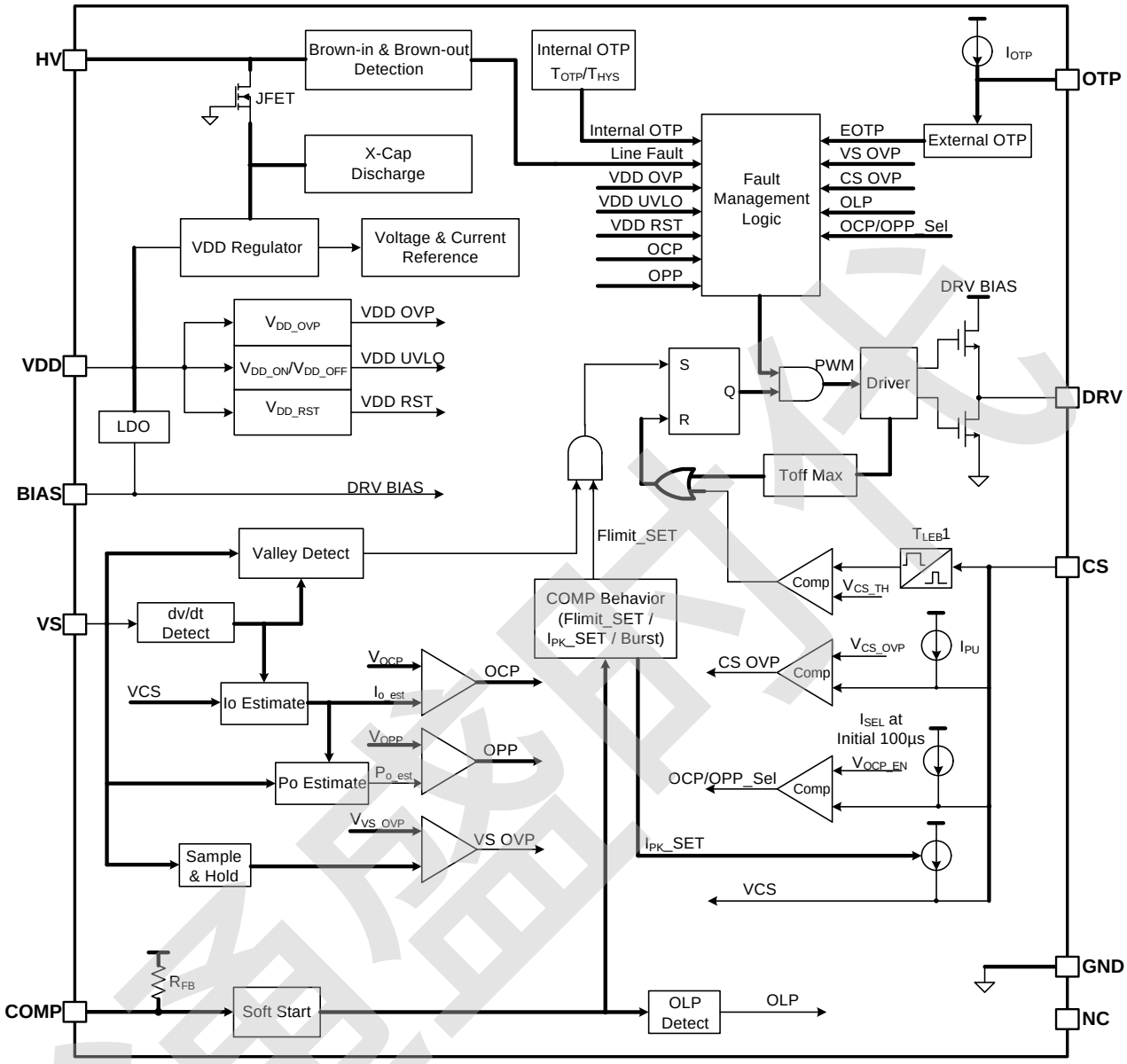
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW1515HA is an offline flyback controller with secondary side feedback, which features multi-mode quasi-resonant (QR) operation. The Quasi- Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

The JW1515HA has an inherent frequency jittering mechanism to improve EMI performance under QR operation.

1. Start-Up

1.1. HV Start-Up

When HV is connected to a rectified AC input, the internal JFET turns on and a HV current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold V_{DD_ON}, the internal startup circuit is disabled. The controller is enabled and the converter starts switching.

1.2 Soft-Start

In the absence of a detected fault, the controller begins to work normally along with soft start. The internal soft-start time is within 4 ms with the feedback signal V_{COMP} rising gradually from minimum level to maximum level. Every restart up is followed by a soft start.

2. Normal Operation

After the controller start-up, it enters normal operation. The JW1515HA realizes output adjustment based on the feedback signal transmitting to the primary-side controller by an opto-coupler.

The JW1515HA is a multi-mode QR controller with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to f_{max} for medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When load is further reduced, switching frequency is fixed at f_{min} along with primary peak current varying from 50% to 25% of its maximum value. When the system is working under very light load condition, the control mode of IC changes to burst mode. When the voltage of COMP pin drops below V_{BUR_L} (0.5V typically), the drive stops. The drive will resume when the voltage of COMP pin rises back to V_{BUR_H} (0.6V typically). Otherwise the gate driver remains at off state to minimize switching loss and reduce standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, V_{COMP}.

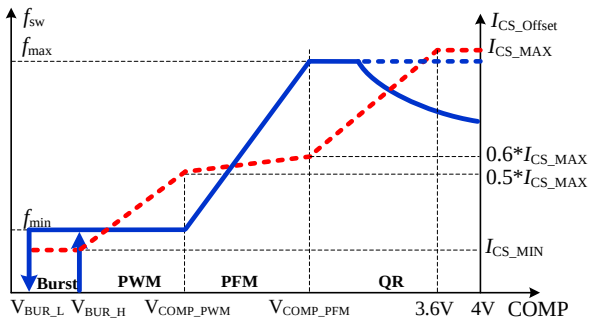


Fig.1 Frequency & Ipk modulation

3. Other Functions and Features

3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JW1515HA. The frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Lead Edge Blanking (LEB)

In order to avoid premature termination of switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the input terminal of an internal current comparator. The current comparator is disabled and can't turn off the external GaN during the blanking time. Fig.2 shows the leading edge blanking time.

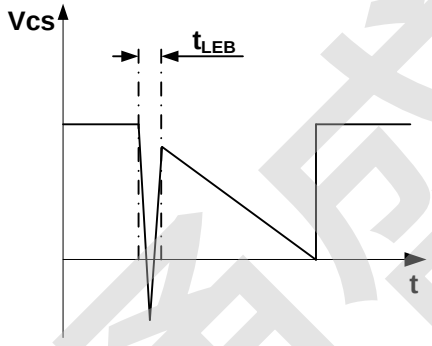


Fig.2 LEB blanking

3.3 CCM Preventing

For JW1515HA, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after a T_{S_MAX} to make sure the system operates in DCM.

3.4 HV Discharge Function

Safety standards such as UL62368 require that any X-capacitors in EMI filters on the AC side of the bridge rectifier quickly discharge to a safe level when AC is disconnected. The standards require that the voltage across the X-cap decay with a maximum time constant of 2s. Typically, this requirement is achieved by including a resistive discharge element in parallel with the X-cap. However, this resistance causes a continuous power dissipation that impacts the standby power performance.

In order to reduce standby power and eliminate the standing loss associated with the conventional discharge resistors, the JW1515HA incorporates X-cap discharge circuit. This circuit periodically monitors the voltage across the X-cap to detect any possibility that AC source disconnection has occurred, and then discharges the voltage across the X-cap using the internal HV current source. The HV discharge function discharges the X-cap to the safety-voltage level in 2s. Fig.3 shows the X-cap discharge timing diagram.

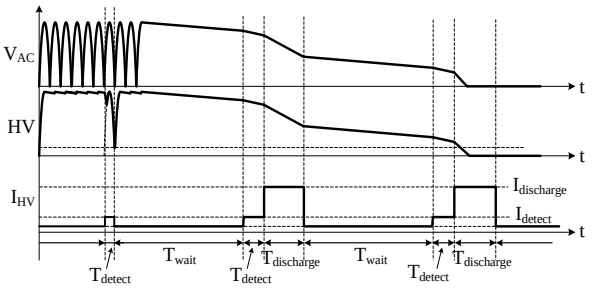


Fig.3 X-cap Discharge

3.5 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be

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set to vary with Ipk. Ensure that the secondary side conduction time is greater than the VS Blanking Time.

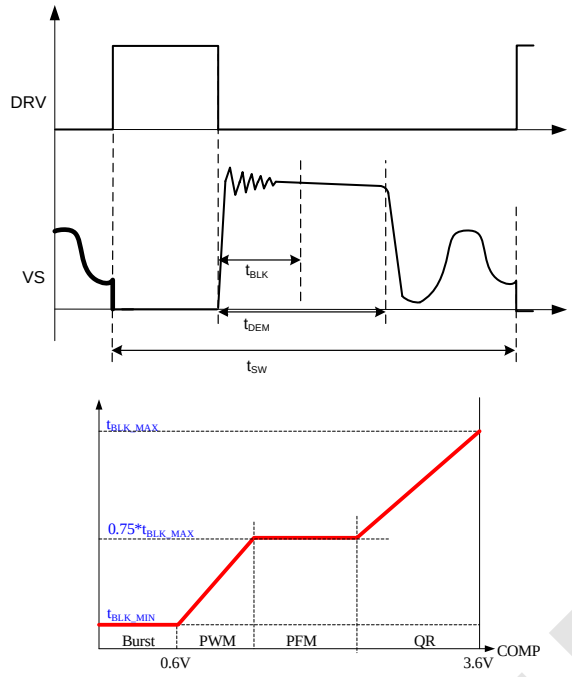

Fig.4 VS blanking time

4. Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above V_{CS_OVP} (2V typically), a CS pin open fault triggered

4.2 Input Brown in / Brown out

The JW1515HA senses HV voltage to realize brown in/out function. When HV voltage is higher than V_{BR_IN} (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit V_{DD_OFF}. When VDD reaches V_{DD_ON} again, the controller starts switching. And the controller is disabled when HV voltage is lower than V_{BR_OUT} (98V typically) for brown-out blanking time (70ms typically). The blanking time is set long enough to ignore a two cycle drop out. The timer starts counting once HV voltage drops below V_{BR_OUT}.

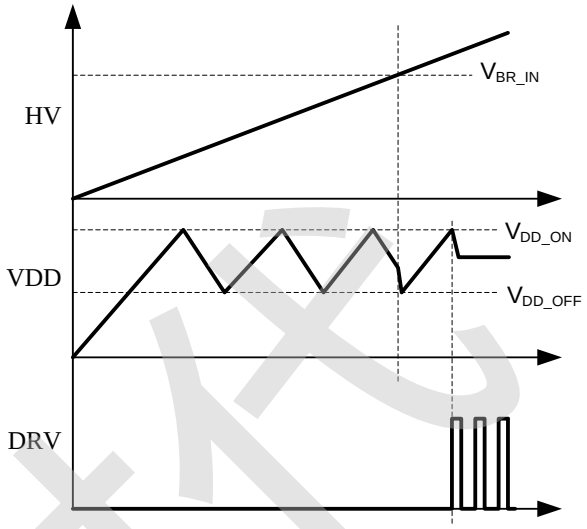

Fig.5 HV Brown-In

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds V_{VS_OVP} for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

4.4 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage differs much. So OCP should be disabled, and the alternative OPP is enabled. The JW1515HA senses CS voltage at initial start to determine whether to use OCP or OPP function as Fig.6 shows. At the initial 100us, an OCP/OPP selection current I_{SEL} (100uA, typically) is applied to CS pin. If CS voltage exceeds a preset enable threshold (typical 0.65V), OPP is enabled and OCP is disabled. Otherwise, OCP is enabled and OPP is disabled.

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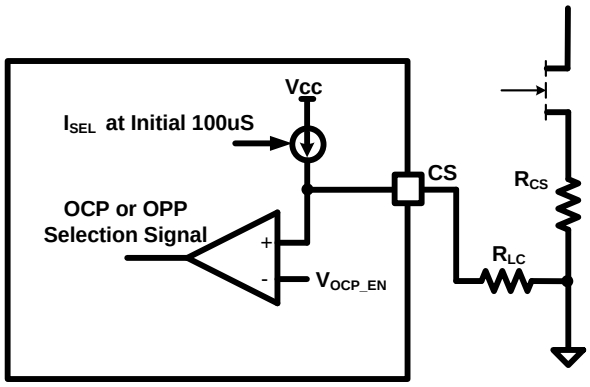

Fig.6 OCP or OPP selection circuit

4.5 OCP

If OCP is enabled, JW1515HA compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the peak inductor current (I_{pk}) is sampled and hold for output current calculation.

As shown in Fig.7, it calculates output current based on secondary side current conduction time t_{ons} and primary side current information V_{CS}. If the calculated output current signal, I_{o_est} is higher than the internal OCP threshold V_{OCP} (0.2V typically) for an OCP blanking time t_{OCP_BLK}, IC enters OCP protection.

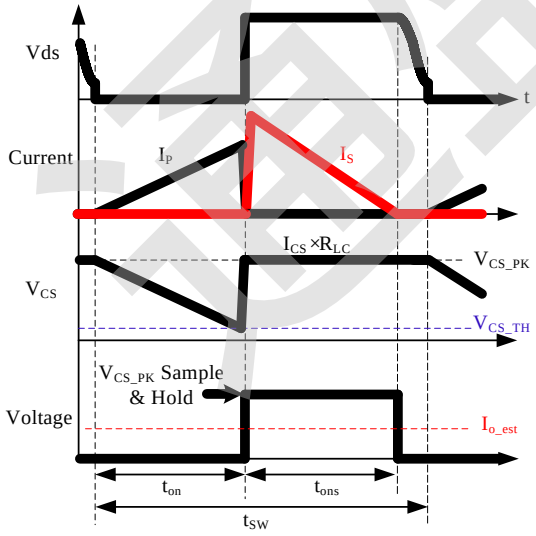

Fig.7 Output current estimation

So the OCP point can be set as:

$$I_{OCP} = \frac{V_{OCP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_S} \quad (1)$$

wherein, N_P is the turns number of primary winding, N_S is the turns number of secondary winding, R_{CS} is the current sensing resistance.

When an OCP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.6 OPP

If OPP is enabled, JW1515HA compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to the VS voltage. So the output power can be expressed as:

$$P_{o\_est} = \frac{V_{CS\_PK} - V_{CS\_TH}}{2R_{CS}} \cdot \frac{N_P}{N_S} \cdot \frac{t_{ons}}{t_{SW}} \cdot \frac{V_S \cdot N_S}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (2)$$

And the OPP point can be set as:

$$P_{OPP} = \frac{V_{OPP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (3)$$

wherein, N_{aux} is the turns number of auxiliary winding, N_P is the turns number of primary winding.

If the calculated output power signal is higher than the internal OPP threshold V_{OPP} (0.8V typically) for an OPP blanking timer t_{OPP_BLK}, IC enters OPP protection. When an OPP fault is

asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.7 Over Load Protection

If the voltage on COMP pin continues exceeds the over-load protection threshold (3.7V typically) more than an OLP blanking time t_{OLP_BLK}, an OLP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.8 VDD OVP

If the voltage on VDD pin continues exceeds the over-voltage protection threshold (90V typically) more than 100us, a VDD OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.9 External OTP

An external NTC resistor (R_{NTC}) is coupled to the OTP pin to program a thermal shutdown temperature. The OTP shutdown threshold is V_{OTP_IN} with an internal pull-up current I_{OTP} (25uA, typically) flowing through R_{NTC}. Once the thermistor is lower than V_{OTP_IN}/I_{OTP}, an OTP fault triggered, and the V_{OTP_IN} threshold is increased to V_{OTP_OUT} (0.5V typically). The OTP resistance will increase to above V_{OTP_OUT}/I_{OTP} to leave OTP. If user needs to disable this function, a 30kΩ resistor can be used to ensure that the OTP can not be triggered.

4.10 Internal OTP

The internal over temperature protection threshold is T_{OTP} (140°C typically). If the junction temperature of the device reaches this threshold, the device shuts down. Since the OTP hysteresis is 30°C typically, when the junction temperature falls below 110°C, the device initiates the UVLO reset and re-start fault cycle.

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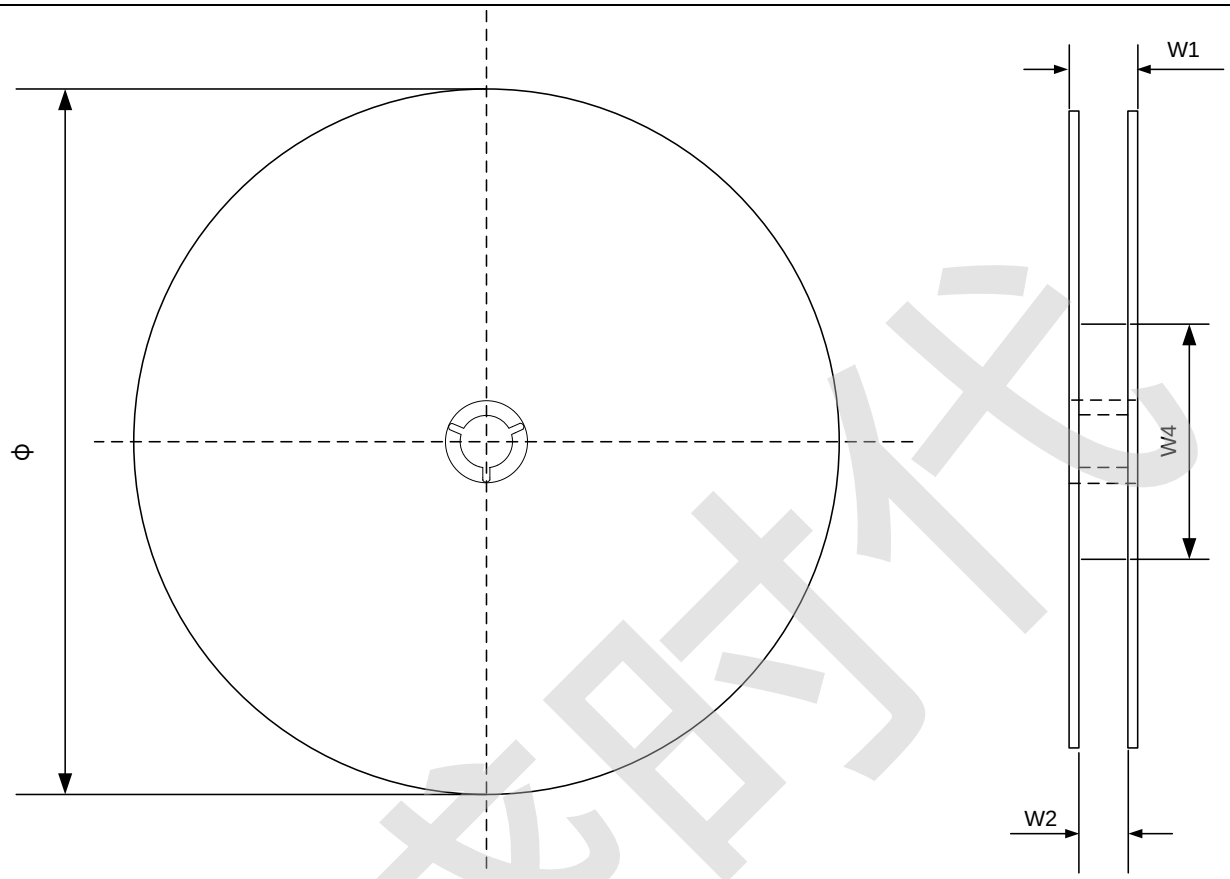
TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
SSOP10	330±2	17.6±2	12.4±2	100±2

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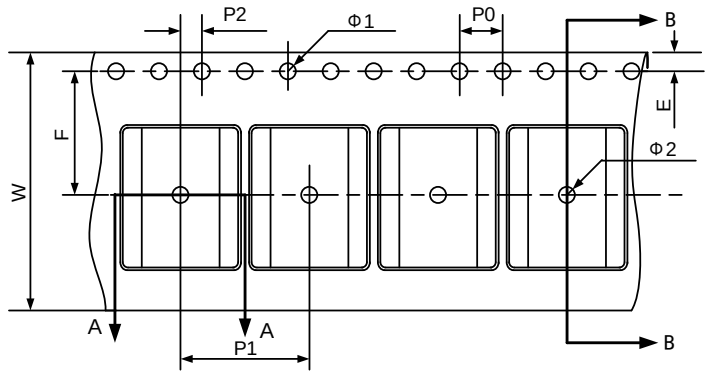
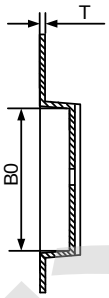
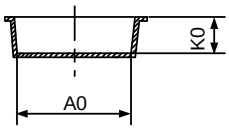
Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

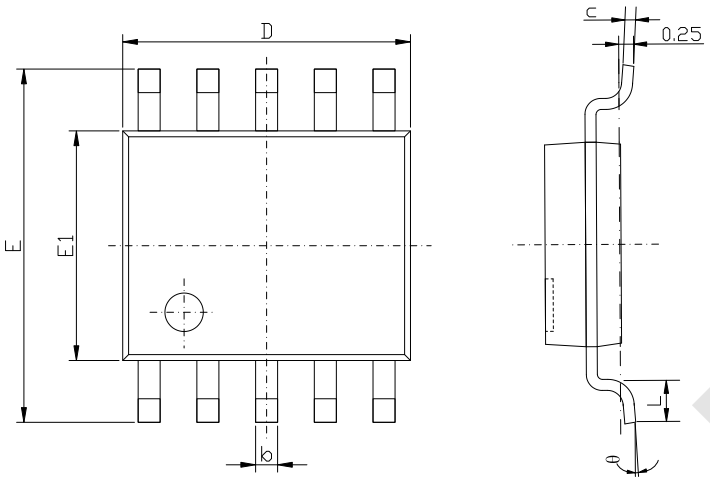
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

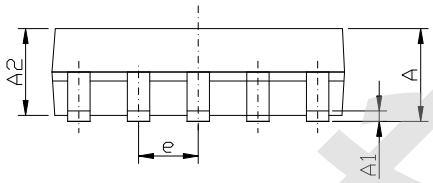
Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
SSOP10	4.0±0.1	2.0±0.1	8.0±0.1	6.40±0.2	5.40±0.2	12.0±0.3	0.25±0.10	2.10±0.1	1.5±0.10	1.5±0.25	1.75±0.1	5.50±0.10

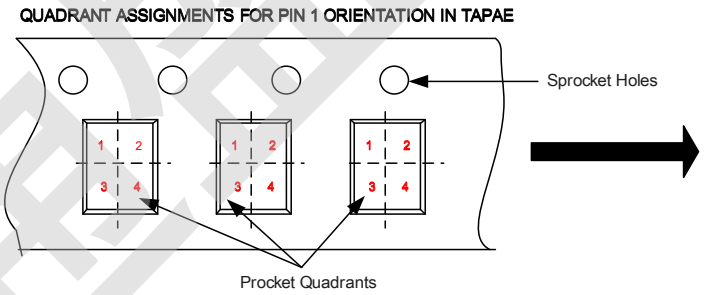
PACKAGE OUTLINE

SSOP10 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.100	0.170	0.250
A2	1.300	—	1.550
b	0.300	—	0.470
c	0.170	0.210	0.250
D	4.700	4.900	5.100
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.000 (TYP)		
L	0.400	—	1.270
θ	0 °	—	8 °





Package Type	Pin1 Quadrant
SSOP10	1

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