JW1520D

CC/CV Flyback Power Switch

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW1520D is an offline CV and CC Flyback power switch with primary-side regulation (PSR), which features quasi-resonant (QR) operation for all operation modes. QR control improves efficiency by reducing the switching loss and also benefits EMI performance with nature frequency variation. The JW1520D combines PWM and PFM control at different input and load condition for highest average efficiency.

JW1520D has internal HV current source for startup to eliminate conventional startup resistor and save standby mode energy consumption, it can comply with the most stringent efficiency regulations such as Energy Star's 5-Star Level and CoC Tier II specifications.

JW1520D offers primary side accurate constant voltage and constant output current regulation, it also eliminates the need for external loop compensation components.

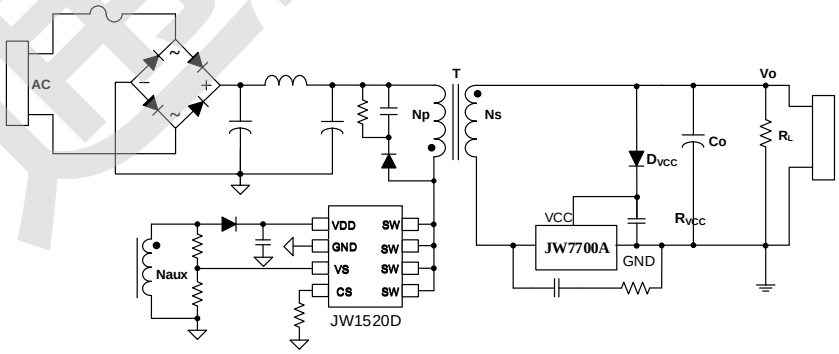
FEATURES

- Integrated with 650V MOSFET
- Tight PSR CC/CV Regulation
- Built-In High-Voltage Startup
- Wider VDD Operation Range
- QR Operation for High Efficiency
- Maximum 85kHz Switching Frequency
- Internal CC/CV Loop Compensation
- Internal Cable Compensation
- Programmable Line Compensation
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP/UVP, Brown-In and Brown-Out, OTP, CS Open and SCP Protection
- SOP-8 package

APPLICATIONS

- Battery Chargers for Cellular Phones
- AC/DC Power Adapter
- Standby and Auxiliary Power Supplies

TYPICAL APPLICATION



Typical application circuit with AC/DC

电话:0755-83387360 手机：13826508770（王先生） 邮箱: 3007605919@qq.com 网址：www.sztssd.com 地址:深圳市福田区中航路鼎诚国际南座18楼1814室

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1520DSOPB#TR	SOP8	JW1520D YW□□□□□	Green

Notes:

1) JW□□□□#TR
- #TR: Tape and Reel (If TR is not shown, it means Tube)
- □□□□: Package Code
- JW: Part No.

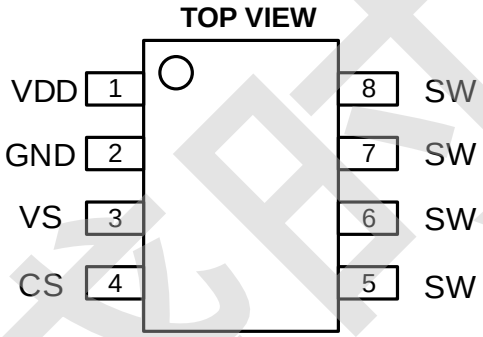
2) Line1: JW □□□□
- □□□□: Product code
- JW: JoulWatt LOGO

Line2: YW □□□□□
- □□□□□: Lot number
- YW: Week code, Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



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ABSOLUTE MAXIMUM RATING[1)]

Rating	Symbol	Value	Unit
Power Switch and Startup Circuits Voltage	V_{DRAIN}	-0.3 to 650	V
Power Switch Current	I_{DRAIN}	4.0	A
V_{DD} Voltage Range	V_{CC}	-0.3 to 35	V
All Other Inputs/Outputs Voltage Range	V_{IO}	-0.3 to 5	V
Maximum Power Dissipation	PD	1.04	W
Maximum Operating Junction Temperature[2) 3)]	T_J	-40 to 150	ºC
Lead Temperature	T_L	260	ºC
Storage Temperature	T_{stg}	-55 to 150	ºC
ESD Capability (Human Body Model)		≥2000	V
ESD Capability (Charge Device Model)		≥500	V

RECOMMENDED OPERATING CONDITIONS

VDD Voltage.....9 to 27V
Operation Junction temperature[2)] ..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	$\theta_{JC(TOP)}$
SOP-8	96	45ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1520D includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values shown are for T_J = 25°C, unless otherwise stated
Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	TYP.	Max.	Units
High Voltage Section						
Supply Current from HV Pin	I_{HV}	V_{HV}=120 V, V_{DD}=0V	-	2.2	3.4	mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=500 V, V_{DD}=V_{DD_ON}-0.2V	-	12	40	uA
Supply Voltage Section						
Turn-On Threshold Voltage	V_{DD_ON}	VDD Rising	15.0	16.5	18.0	V
AZTurn-Off Threshold Voltage	V_{DD_OFF}	VDD Falling	7.4	8	8.6	V
Threshold Voltage for Latch Release	V_{DD_DLH}	VDD Falling	3.7	4.2	4.6	V
Startup Current	I_{DD_ST1}	V_{DD}=V_{DD_ON}-0.16V	-	305	360	uA
	I_{DD_ST2}	V_{DD}=V_{DD_OFF}-1V	-	-	50	uA
Operating Supply Current	I_{DD_OP}	V_{DD}=15 V, DRV=1nF, F_{SW}=85kHz	-	-	1.38	mA
VDD OVP Voltage	V_{DD_OVP}	VDD Rising	27	28.4	29.8	V
Voltage-Sense Section						
Maximum VS Source Current Capability	I_{VS_MAX}		-	-	5	mA
VS Source Current threshold for Brown-In	I_{VS_BI}		70	120	170	uA
VS Source Current threshold for Brown-Out[5)]	I_{VS_BO}		-	60	-	uA
Line Voltage Compensation Coefficient[5)]	K_{LC}	I_{VS}/I_{CS}	-	110	-	
Cable Compensation Coefficient[5)]	K_1			11.8		uA/V
Blanking time for VS Sampling[5)]	T_{VS_BLK1}	V_{CS}=V_{CS_MIN}	-15%	2.1	+15%	uS
	T_{VS_BLK2}	V_{CS}=V_{CS_MAX}	-15%	5.3	+15%	uS
Output Voltage Reference	V_{REF_CV}		-1.5%	2.31	+1.5%	V
Output OVP threshold	V_{VS_OVP}		-5%	2.9	+5%	V
Output UVP threshold	V_{VS_UVP}		-5%	1.45	+5%	V
Output OVP/UVP Debounce Cycle Counts[6)]	N_{VS_OVP}		-	3	-	Cycle
Output UVP Blanking Time at start-up[6)]	T_{VS_UVP}		-20%	95	+20%	mS
Current-Sense Section						
Max CS Threshold Voltage	V_{CS_MAX}		-5%	0.58	5%	V
Min CS Threshold Voltage	V_{CS_MIN}		-5%	0.18	+5%	V
Internal CC Reference	V_{REF_CC}		-3%	0.275	+3%	V

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Primary OCP threshold	V_{SCP}		1.1	1.2	1.3	V
Leading-Edge Blanking Time[5)]	T_{LEB}		-	320	-	nS
Frequency Section						
Minimum ON Time[6)]	T_{ON_MIN}		-	360	-	nS
Frequency Jittering[5)]	ΔF_{OSC}		-	±8	-	%
Maximum Switching frequency	F_{MAX}		77	84.5	90	KHz
Minimum Switching frequency	F_{MIN}		336	390	444	Hz
Over Temperature Protection						
Thermal Shutdown Threshold [6)]	T_{OTP}		135	145	155	°C
Thermal Shutdown Hysteresis [6)]	T_{HYS}		-	30	-	°C
Power MOSFET Section						
Breakdown Voltage	V_{BR}		650	-	-	V
MOS R_{DS_ON}	R_{DS_ON}		-	2.3	2.6	Ohm
Input Capacitance	C_{ISS}		-	550	-	pF
Output Capacitance	C_{OSS}		-	56	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	4.5	-	pF

Note：

5) Guaranteed by Design.

6) Derived from bench characterization. Not tested in production.

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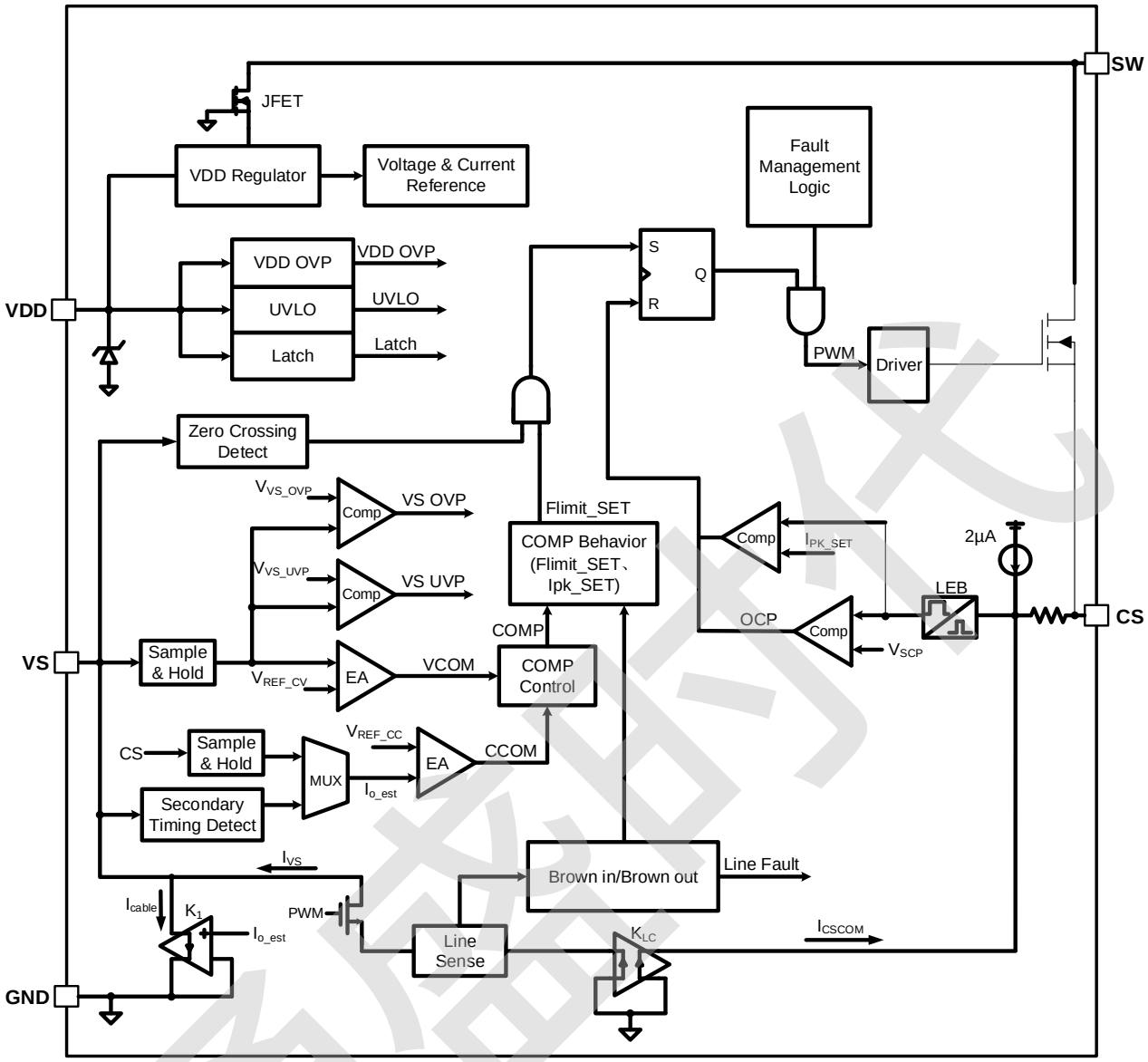
PIN DESCRIPTION

PIN SOP-8	NAME	DESCRIPTION
1	VDD	Power supply pin of both analog and gate driver of IC. Connect a cap to GND.
2	GND	The Ground of the IC
3	VS	Voltage sensing input pin. connect to auxiliary winding through a resistor divider. The pin sense the output voltage for OVP and UVP protection, it also detects the resonant valley to implement QR operation. This pin is also used for brown-in, brown-out protection and peak current compensation caused by internal delay. Besides, this pin is used for output cable drop compensation.
4	CS	Current sense input pin. This pin sense the primary switch current for peak current mode control and output current estimation. The estimated output current is used for primary side CC control and cable compensation. Also, CS pin has an internal current limit for primary side OCP.
5,6,7,8	SW	The drain of inner power MOSFET

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW1520D is an offline Flyback power switch features multi-mode quasi-resonant (QR) operation. The Quasi-Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

It offers accurate primary side constant voltage and current regulation. JW1520D has an inherent frequency quiver mechanism to improve the EMI performance under QR operation.

1. Start-Up

1.1. HV Start-Up

The internal JFET turns on and a HV current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold V_{DD_ON}, the internal startup circuit is disabled. The controller is enabled and the converter starts switching.

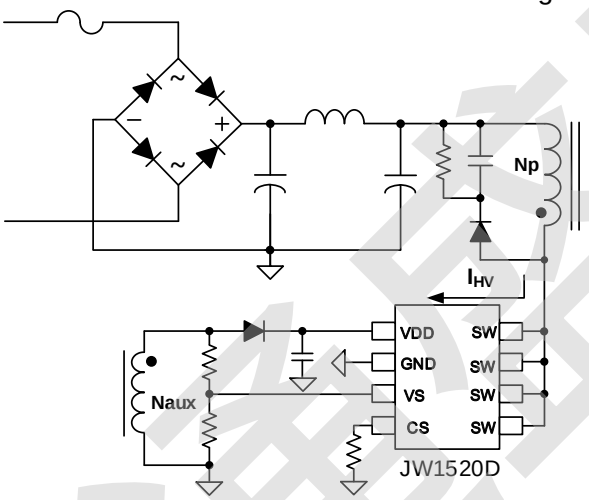


Figure 1. HV Start-Up

1.2 Initial Power On

After the controller is enabled, it outputs three cycles with primary side peak current limited to V_{CS_MIN}. It is used sensing any input and output fault with minimal power delivery. The VS pin is clamped to GND during MOS on time. The bulk capacitor voltage is sensed by the current flowing out of the VS pin (the up resistance of the divider). During the first three pulse, it should be always above the threshold I_{VS_BI}. If it does not, then switching stops and the UVLO reset and the controller enters re-start mode. Once running, it must drop below the stop threshold I_{VS_BO}, for three consecutive cycles to initiate the brown out fault response.

2. Normal Operation

After the controller start-up, if there is no fault detected, it enters normal operation. The output current and voltage are both regulated at the primary side.

There are two loops for CC/CV control, one is the current loop which controls the output current via primary side constant current regulation, and the other is the voltage loop which regulates output voltage based on sampled output voltage information on the primary side during flyback period.

2.1 CV Mode Operation

For primary side control, the output voltage is sensed on the auxiliary winding when the magnetizing current transferred to the secondary side.

2.1.1 Voltage Sensing

To achieve accurate representation of the output voltage on the auxiliary winding, the output voltage should be sampled when the secondary winding current reaches zero, as shown in Figure 2. The internal reference of output voltage is V_{REF_CV}. The resistor divider can be designed with selected turns ratio for desired output voltage.

$$V_{out} = V_{REF\_CV} \cdot K_s \cdot \frac{R_{up}+R_{down}}{R_{down}} \cdot \frac{N_s}{N_{aux}} \quad (1)$$

Where, V_{REF_CV} is the internal voltage reference for CV operation, K_s is sampling coefficient depends on the resonance characteristic of the circuit, 1.05 (typ), Ns is the turns number of secondary winding, Naux is the turns number of auxiliary winding,

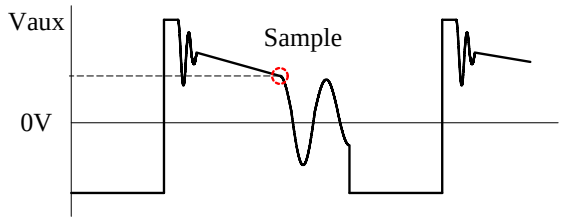


Figure 2. Primary Side Voltage Sensing

2.1.2 Operating Modes

During CV mode, according to the internal control-law voltage, COMP, the converter operates in different modes for efficiency optimization. Figure 3 illustrates the frequency modulation modes during CV mode. It can be divided into four operation regions, as shown in Figure 3:

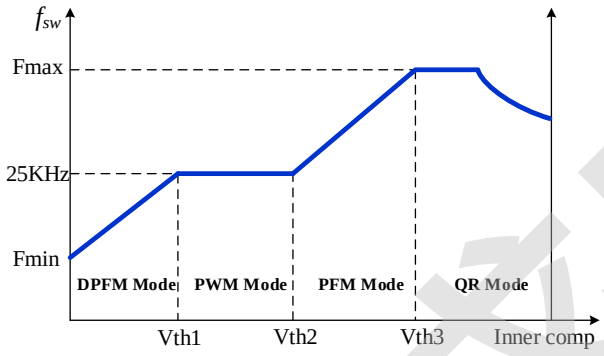


Figure 3. Frequency Modulation During CV Mode

Under heavy load condition, the system operates in QR mode. For medium-load range, the frequency modulation (PFM) is used and primary peak current is fixed to achieve excellent regulation and high efficiency. When the load is further reduced, switching frequency is fixed at nominal 25KHz. When the system is near zero loading, the IC operates in Deep PFM mode. In this way, the no-load consumption can be less than 40mW. Transitions between levels are automatically accomplished by the controller depending on the internal control-law voltage, COMP.

When system enters overload condition, the output voltage drops and the VS sampled voltage should be lower than V_{REF_CV} internal reference which makes system enter CC Mode automatically.

2.2 CC Mode Operation

The maximum output average current is regulated at the primary side.

2.2.1 Output Current Calculation

At the end of the primary switch turns off, the peak inductor current is sampled and hold for output current calculation.

As shown in Figure 4, the current loop calculates output current based on secondary side current conduction time T_{ons} and primary side current information V_{CS}.

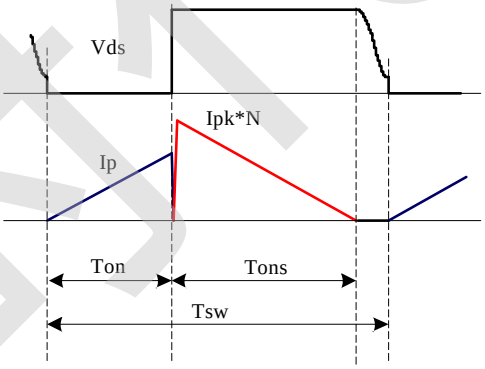


Figure.4 Output Current Estimation

The output current can be set as:

$$I_o = \frac{V_{REF\_CC} \cdot N}{2 \cdot R_{cs}} \quad (2)$$

Where N is the transformer turns ratio. R_{CS} is the current sensing resistance. V_{REF_CC} is the internal current reference for CC operation.

2.2.2 Line Voltage Compensation

The peak current is larger with the input voltage rising due to the switch turn-off delay. And the accuracy of CC control is related to the accuracy of peak current. To improve the accuracy of CC control, JW1520D integrate line voltage compensation function.

3. Other Functions And Features

3.1 Frequency Quiver For EMI

To achieve good EMI performance, frequency quiver method is integrated in JW1520D.The frequency is no-fixed and varied by ΔF_{OSC} around its normal value.

3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS Pin and the current comparator input. The current comparator is disabled and can't turn off the external MOSFET during the blanking time. Figure 5 shows the leading-edge blanking.

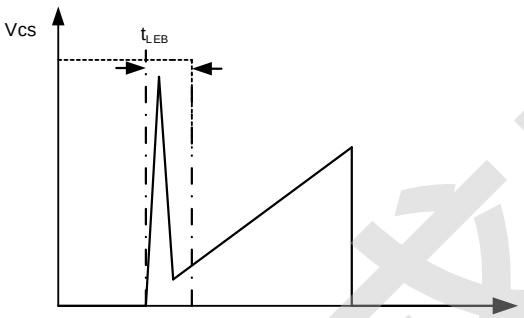


Figure.5 The Leading-Edge Blanking

3.3 Cable Drop Compensation (CDC)

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In JW1520D, an offset voltage is generated at VS pin by an internal current source flowing out of the upper resistor, as shown in Figure 6. The current is proportional to the output current calculation I_{o_est}, thus, it is inversely proportional to the output power. Therefore, the drop due the cable loss can be compensated.

By adjusting the resistance of Rup, the cable loss compensation can be programmed. The maximum CDC voltage is given by:

$$V_{Cable} = 3 \cdot K_1 \cdot I_{o\_est} \cdot R_{up} \cdot \frac{N_s}{N_{aux}} \qquad (3)$$

Where, Ns is the turns number of secondary winding, K_1 is current factor, 10uA/V. When the output current is maximum, the I_{O_EST} is up to maximum and is equal to V_{REF_CC}.

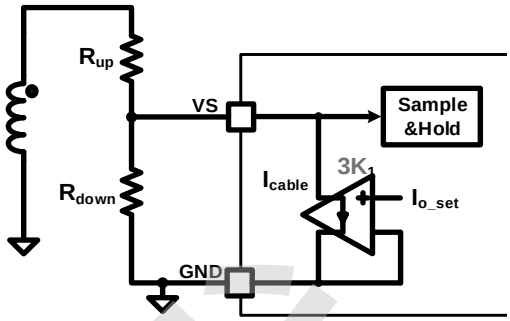


Figure.6 Cable Drop Compensation

4. Protection

4.1 CS Pin Open Protection

The CS pin has a 2-μA minimum pull-up current that brings the CS pin above the V_{SCP} if the CS pin is open. This causes the primary Over-Current fault.

4.2 Primary Side OCP

The JW1520D always operates with cycle-by-cycle primary-peak current control. If the voltage on CS exceeds the V_{SCP}, any time after the internal shorter leading-edge blanking time and before the end of the transformer demagnetization, for three consecutive cycles the device shuts down and the VDD UVLO reset and re-start fault cycle begins.

4.3 Brown In / Brown Out

The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. From the start state, the sensed VS current IVS must exceed the run current threshold, IVS_BI, within the first three cycles after switching starts as VDD reaches VDD_ON. If it does not, then switching stops and the VDD

UVLO reset and re-start fault cycle is initiated. Once running, I_{VS} must drop below the stop level, I_{VS_BO} for three consecutive cycles to initiate the fault response.

4.4 VS OVP

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds V_{VS_OVP}, for three consecutive switching cycles an VS-OVP fault is asserted and the device shuts down and the VDD UVLO reset and re-start fault cycle begins.

4.5 VS UVP

If the voltage sample on VS pin continues below the under-voltage protection threshold, V_{VS_UVP} more than t_{VS_UVP}, an VS UVP fault is asserted and the device shuts down and the VDD UVLO reset and re-start fault cycle begins.

4.6 VDD OVP

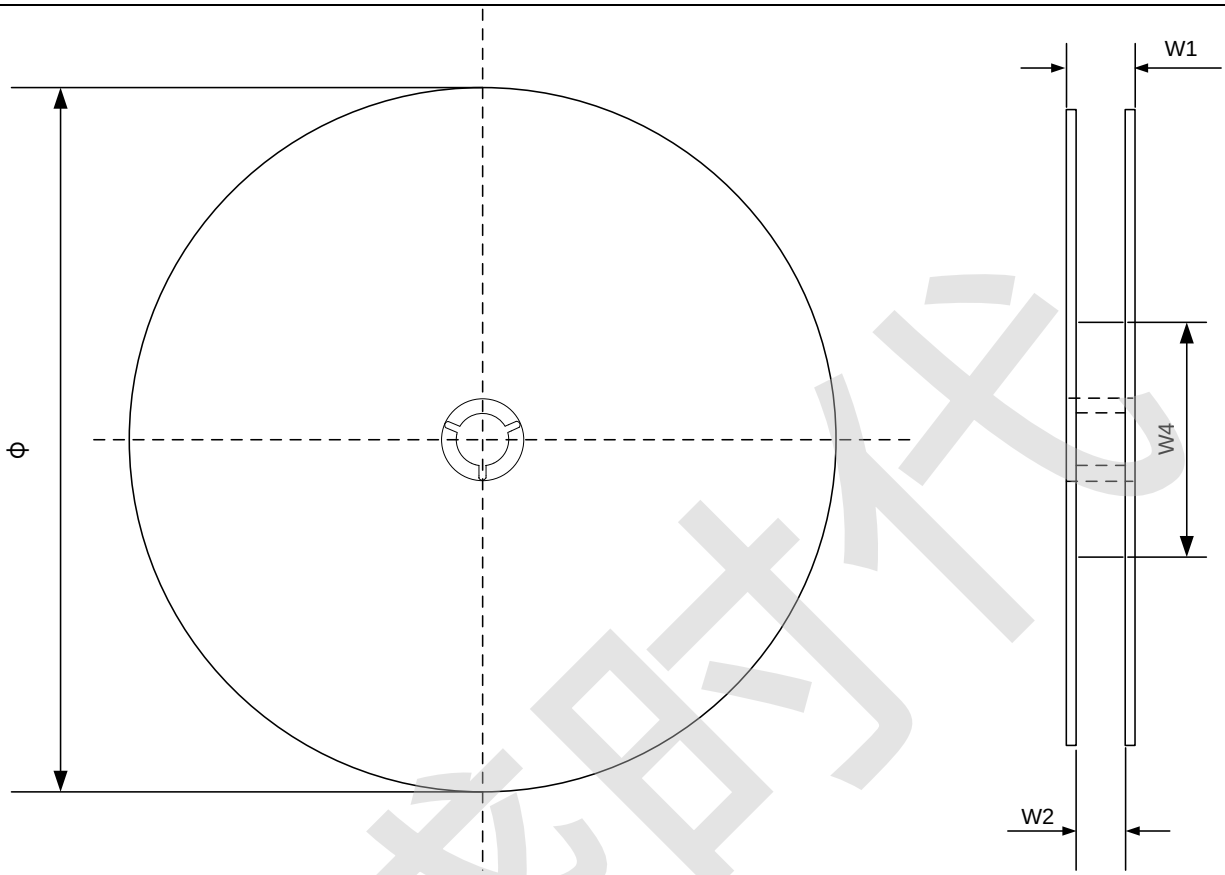
If the voltage on VDD pin continues exceeds the over-voltage protection threshold, V_{DD_OVP} more than 110us, an VDD-OVP fault is asserted. The device shuts down and the VDD UVLO reset and re-start fault cycle begins.

4.7 OTP

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled If the junction temperature exceeds the thermal shutdown threshold, T_{OTP}. The controller restarts once the IC temperature drops below T_{OTP} by the thermal shutdown hysteresis, T_{HYS}. A thermal shutdown fault is cleared if V_{DD} drops below V_{DD_DLH}. A power−up sequence commences at the next V_{DD_ON} if all faults are removed.

TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
SOP-8	330±2	17.6±2	12.4±2	100±2

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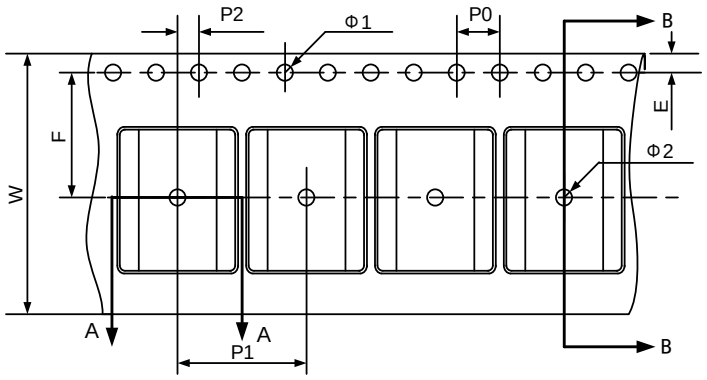
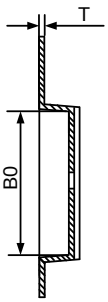
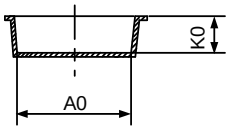
Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

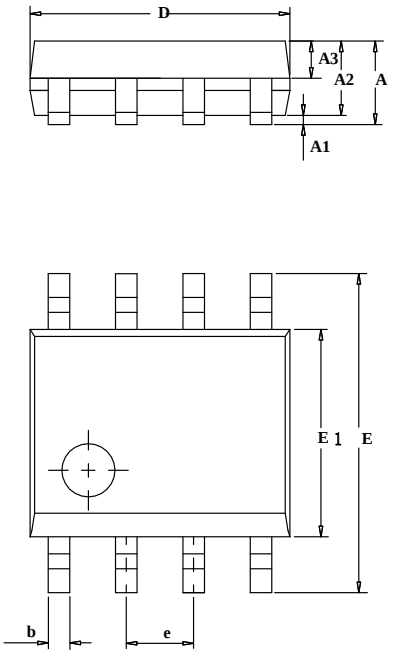
Note :

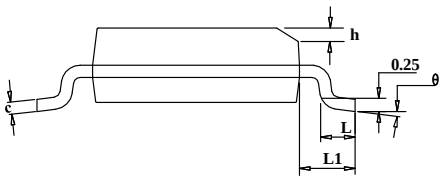
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions(mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
SOP-8	4.0±0.1	2.0±0.1	8.0±0.1	6.40±0.3	5.35±0.3	12.0±0.3	0.25±0.2	2.00±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10

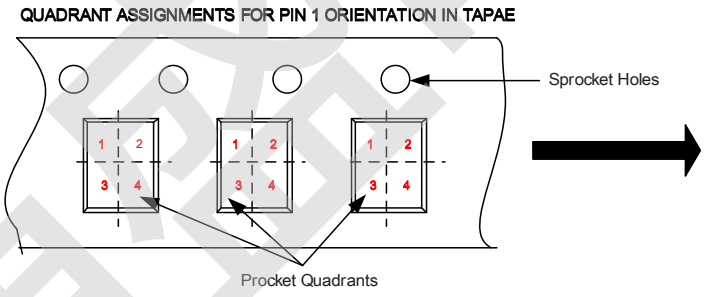
PACKAGE OUTLINE

SOP-8 UNIT: mm





Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
c	0.20	—	0.24
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0°	—	8°



Package Type	Pin1 Quadrant
SOP-8	1

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