

## 1A, Ultra-Low Dropout, Ultra-Fast CMOS LDO Regulator

### General Description

The RT9187 is a high-performance, 1A LDO regulator, offering extremely high PSRR and ultra-low dropout. Ideal for portable RF and wireless applications with demanding performance and space requirements.

A noise reduction pin is also available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The RT9187 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices.

The RT9187 consumes less than 0.1µA in shutdown mode and has fast turn-on time less than 40µs. The other features include ultra-low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the VDFN-8L 3x3 and SOP-8 (Exposed Pad) package.

### Ordering Information

RT9187-(□□)□□

- Package Type
  - QV : VDFN-8L 3x3 (V-Type)
  - SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)
- None : Adjustable Output Fixed Output Voltage Code
  - 10 : 1.0V
  - 11 : 1.1V
  - :
  - 32 : 3.2V
  - 33 : 3.3V
  - 1L : 1.34V

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Features

- Ultra-Low-Noise for RF Application
- Ultra-Fast Response in Line/Load Transient
- Quick Start-Up (Typically 40µs)
- <0.1µA Standby Current When Shutdown
- Low Dropout : 240mV at 1A
- Wide Operating Voltage Ranges : 2.5V to 5.5V
- TTL-Logic-Controlled Shutdown Input
- Current Limiting Protection
- Thermal Shutdown Protection
- Only 2.2µF Output Capacitor Required for Stability
- High Power Supply Rejection Ratio
- RoHS Compliant and 100% Lead (Pb)-Free

### Applications

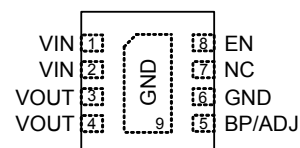
- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Mini PCI & PCI-Express Cards
- PCMCIA & New Cards
- Portable Information Appliances

### Marking Information

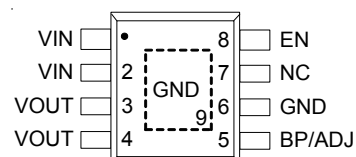
For marking information, contact our sales representative directly or through a RichTek distributor located in your area.

### Pin Configuration

(TOP VIEW)



VDFN-8L 3x3



SOP-8 (Exposed Pad)

## Typical Application Circuit

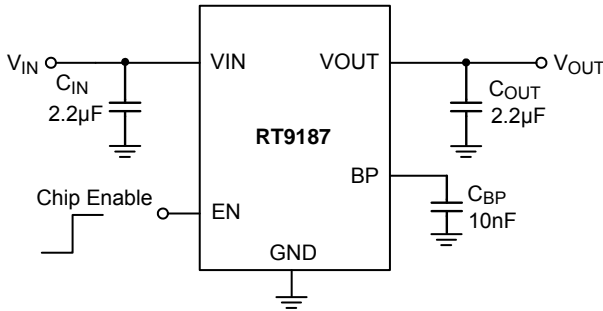


Figure 1. Fixed Operation

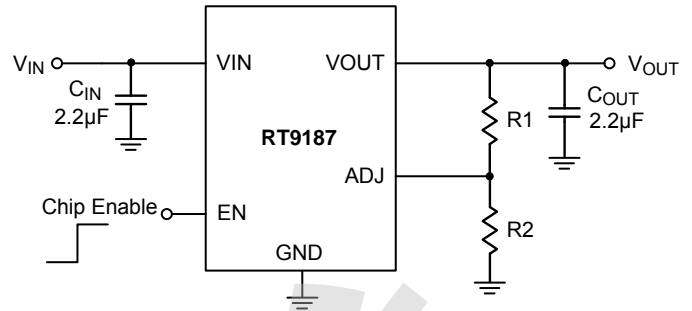


Figure 2. Adjustable Operation

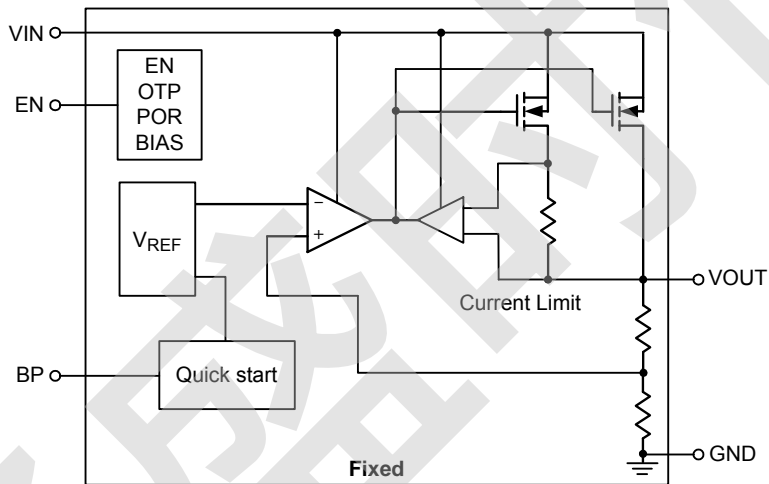
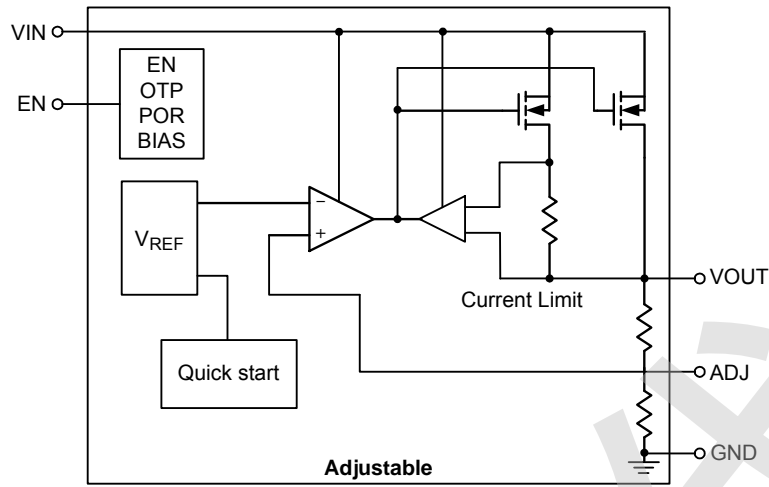
$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) \text{ Volts}$$

**Note :** The value of R2 should be less than 80k to maintain regulation.

## Function Pin Description

Pin No.		Pin Name	Pin Function
Fixed Output Voltage	Adjustable Output Voltage		
1	1	VIN	Supply input.
2	2	VIN	Supply input.
3	3	VOUT	Regulator output.
4	4	VOUT	Regulator output.
5	--	BP	Noise reduction. Connecting a 10nF capacitor to GND to reduce output noise.
--	5	ADJ	If external feedback resistors are applied, the output voltage will be: $V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) V$
6, 9 (Exposed Pad)	6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	7	NC	No internal connection.
8	8	EN	Enable input logic, active high. When the EN goes to a logic low, the device is in shutdown mode.

**Functional Block Diagram**



## Absolute Maximum Ratings (Note 1)

• Supply Input Voltage	6V
• EN Input Voltage	6V
• Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	
VDFN-8L 3x3	1.429W
SOP-8 (Exposed Pad)	1.33W
• Package Thermal Resistance (Note 2)	
VDFN-8L 3x3, $\theta_{JC}$	8.2°C/W
VDFN-8L 3x3, $\theta_{JA}$	70°C/W
SOP-8 (Exposed Pad), $\theta_{JC}$	15°C/W
SOP-8 (Exposed Pad), $\theta_{JA}$	75°C/W
• Lead Temperature (Soldering, 10 sec.)	260°C
• Junction Temperature	150°C
• Storage Temperature Range	-65°C to 150°C
• ESD Susceptibility (Note 3)	
HBM	2kV
MM	200V

## Recommended Operating Conditions (Note 4)

• Supply Input Voltage	2.5V to 5.5V
• EN Input Voltage	0V to 5.5V
• Junction Temperature Range	-40°C to 125°C
• Ambient Temperature Range	-40°C to 85°C

## Electrical Characteristics

( $V_{IN} = V_{OUT} + 1V$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = C_{OUT} = 2.2\mu\text{F}$  (Ceramic) &  $C_{BP} = 10\text{nF}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Output Voltage Accuracy (Fixed Output Voltage)	$\Delta V_{OUT}$	$I_{OUT} = 10\text{mA}$	-1.5	0	1.5	%	
Output Voltage Range (Adjustable)	$V_{OUT\_Adj}$		0.8	--	4.5	V	
Quiescent Current (Note 5)	$I_Q$	$V_{EN} \geq V_{IH}$ , $I_{OUT} = 0\text{mA}$	--	380	500	$\mu\text{A}$	
Standby Current (Note 6)	$I_{STBY}$	$V_{EN} \leq V_{IL}$ , $V_{IN} = 3.3V$	--	0.1	1	$\mu\text{A}$	
Current Limit	$I_{LIM}$	$R_{LOAD} = 0.5\Omega$ , $V_{IN} = 3.3V$	2	2.8	3	A	
Dropout Voltage (Note 7)	$V_{DROP}$	$I_{OUT} = 0.25\text{A}$ (Note 9)	--	60	100	mV	
		$I_{OUT} = 0.5\text{A}$	--	120	180		
		$I_{OUT} = 1.0\text{A}$	--	240	360		
Load Regulation (Note 8) (Fixed Output Voltage)	$\Delta V_{LOAD}$	$V_{IN} = (V_{OUT} + 0.5V)$ $10\text{mA} < I_{OUT} < 1.0\text{A}$	--	0.4	--	%/A	
EN Threshold Voltage	Logic-Low	$V_{IL}$	$V_{IN} = 3.3V$	--	--	0.6	V
	Logic-High	$V_{IH}$	$V_{IN} = 3.3V$	1.2	--	--	
Enable Pin Current	$I_{EN}$	$V_{IN} = 3.3V$ , enable	--	0.1	1	$\mu\text{A}$	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Rejection Rate	f = 100Hz	I <sub>OUT</sub> = 300mA	--	-60	--	dB
	f = 10kHz		--	-50	--	
Line Regulation	ΔV <sub>LINE</sub>	V <sub>IN</sub> = (V <sub>OUT</sub> + 0.5) to 5.5V, I <sub>OUT</sub> = 1mA	--	--	0.3	%
Start-Up Time	T <sub>Start_Up</sub>	R <sub>LOAD</sub> = 3Ω, 1nF ≤ C <sub>BP</sub> ≤ 0.1μF	--	40	--	μs
Thermal Shutdown Temperature	T <sub>SD</sub>		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT <sub>SD</sub>		--	30	--	
<b>ADJ</b>						
Reference Voltage Tolerance	V <sub>REF</sub>		0.784	0.8	0.816	V
ADJ Pin Current	I <sub>ADJ</sub>	V <sub>ADJ</sub> = V <sub>REF</sub>	--	10	100	nA

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** θ<sub>JA</sub> is measured in natural convection at T<sub>A</sub> = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ<sub>JC</sub> is on the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Quiescent, or ground current, is the difference between input and output currents. It is defined by I<sub>Q</sub> = I<sub>IN</sub> - I<sub>OUT</sub> under no load condition (I<sub>OUT</sub> = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

**Note 6.** Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal (V<sub>EN</sub> > 1.8V).

**Note 7.** The dropout voltage is defined as V<sub>IN</sub> - V<sub>OUT</sub>, which is measured when V<sub>OUT</sub> is V<sub>OUT(NORMAL)</sub> - Σ 100mV.

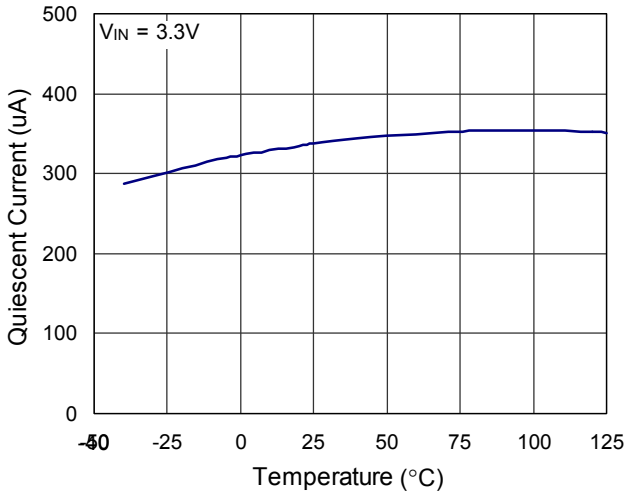
**Note 8.** Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 10mA to 1.0A.

**Note 9.** Performance at -5°C ≤ T<sub>A</sub> ≤ 85°C is assured by design.

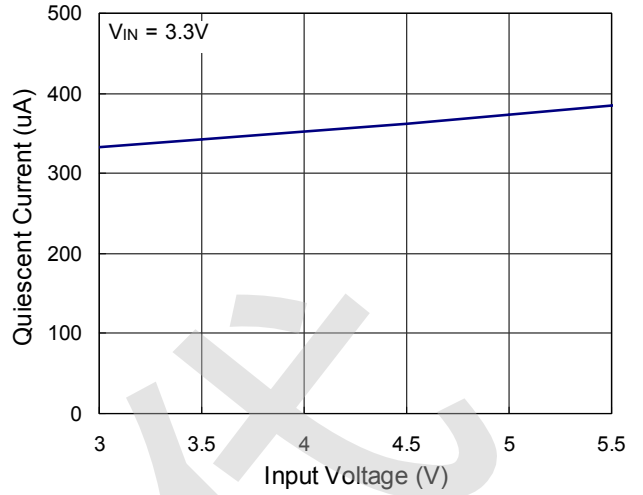
## Typical Operating Characteristics

( $C_{OUT} = 2.2\mu F/5R$ ,  $C_{BP} = 10nF$ , unless otherwise specified)

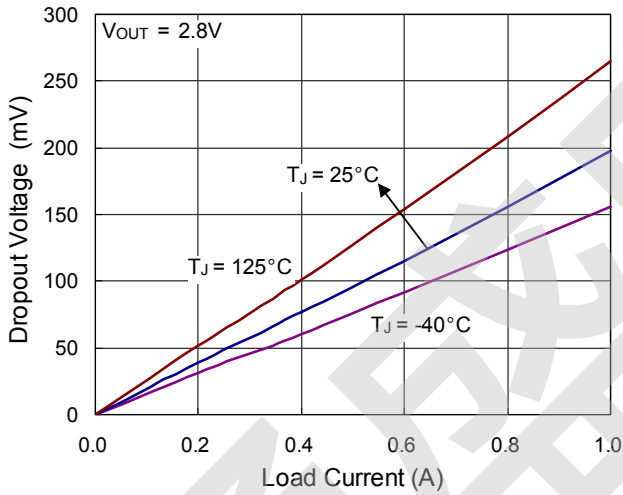
### Quiescent Current vs. Temperature



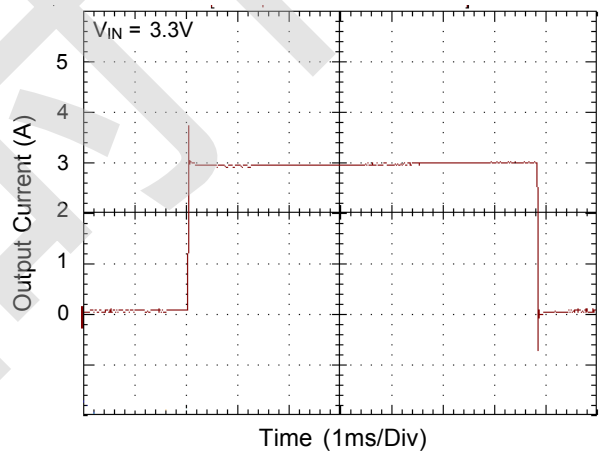
### Quiescent Current vs. Input Voltage



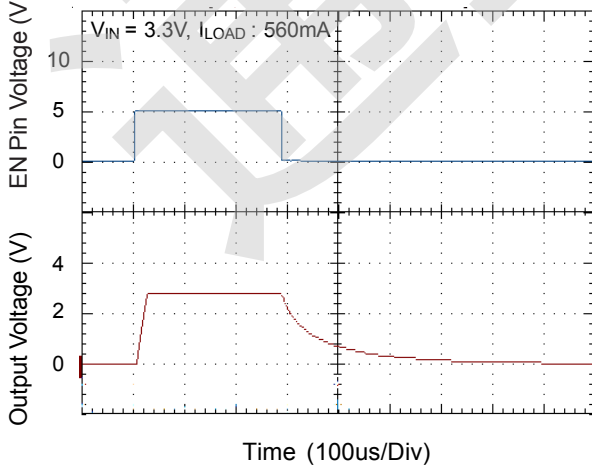
### Dropout Voltage vs. Load Current



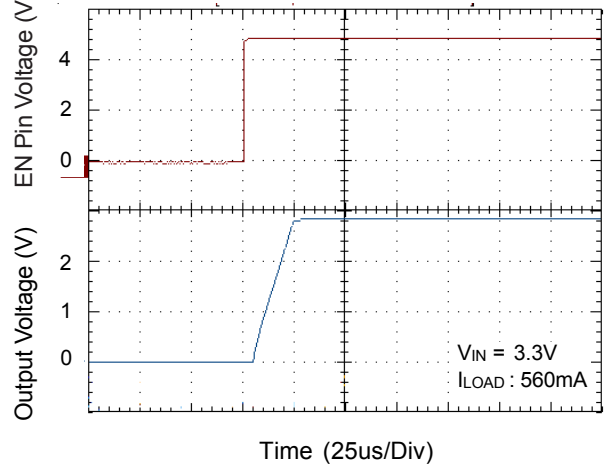
### Current Limit



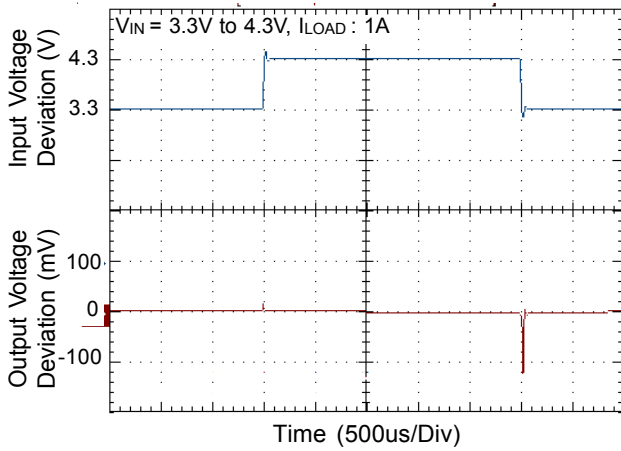
### EN Pin Shutdown Response



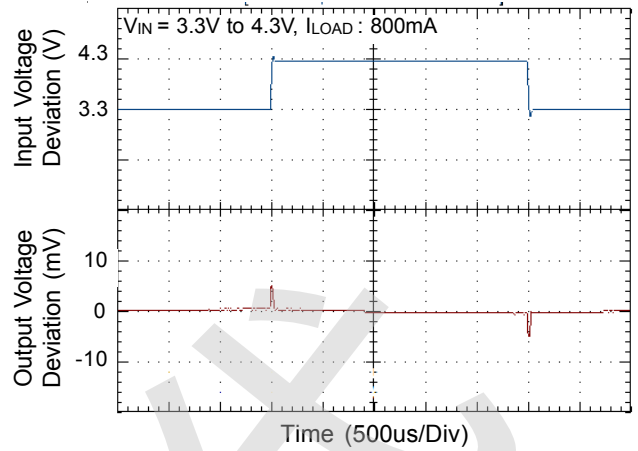
### Start Up



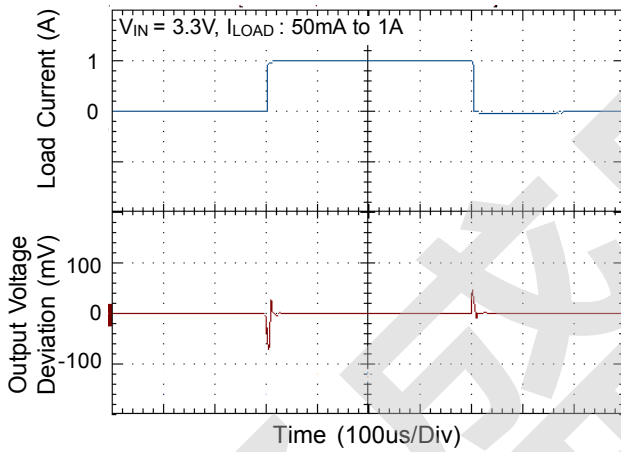
Line Transient Response



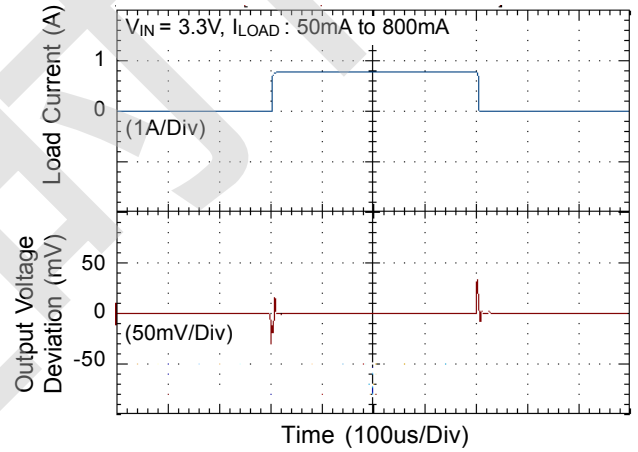
Line Transient Response



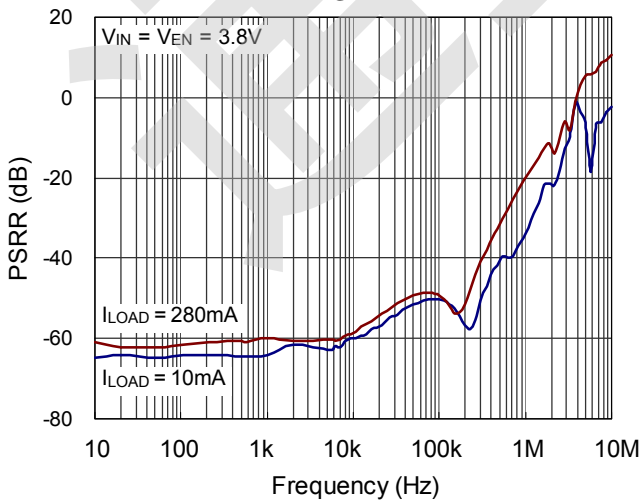
Load Transient Response



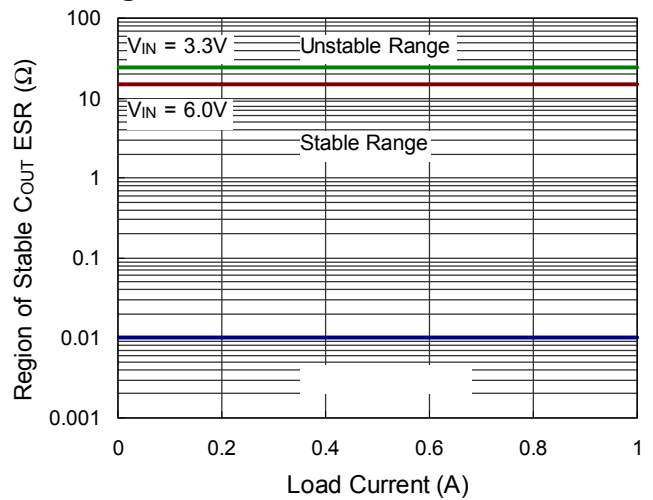
Load Transient Response



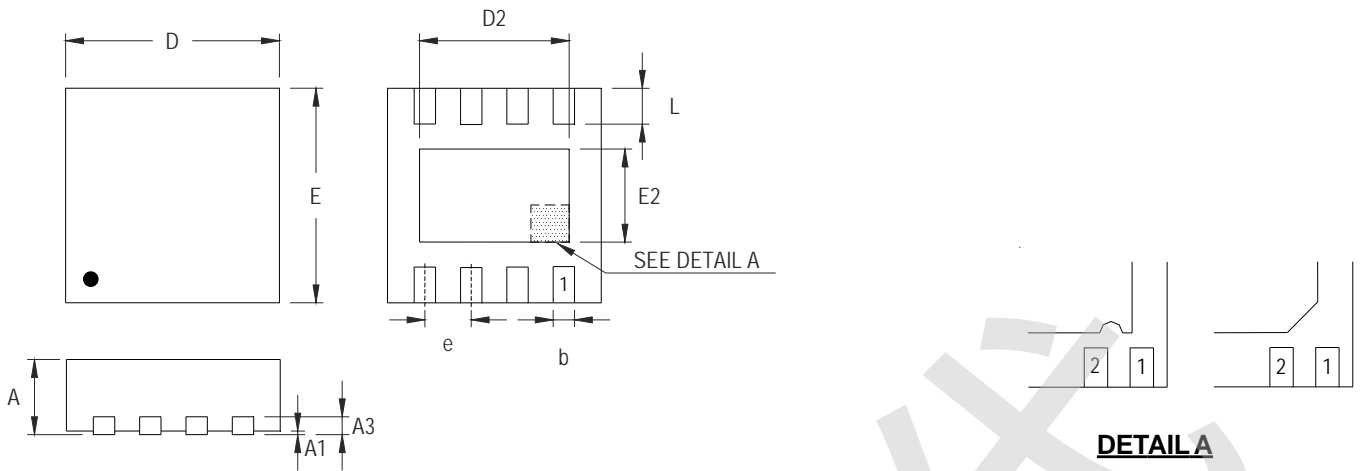
PSRR



Region of Stable  $C_{OUT}$  ESR vs. Load Current



Outline Dimension



**DETAIL A**

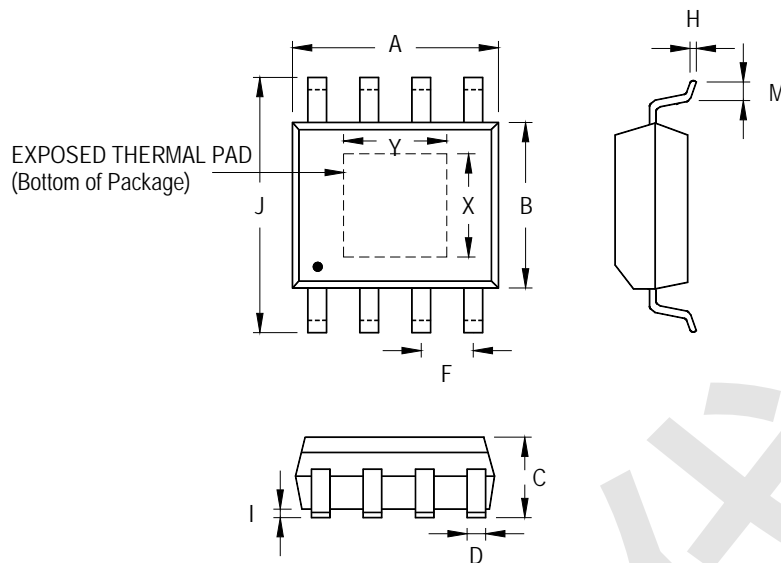
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

V-Type 8L DFN 3x3 Package





Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

**8-Lead SOP (Exposed Pad) Plastic Package**

**Richtek Technology Corporation**

14F, No. 8, Tai Yuen 1<sup>st</sup> Street, Chupei City  
 Hsinchu, Taiwan, R.O.C.  
 Tel: (8863)5526789

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